

Compal Confidential

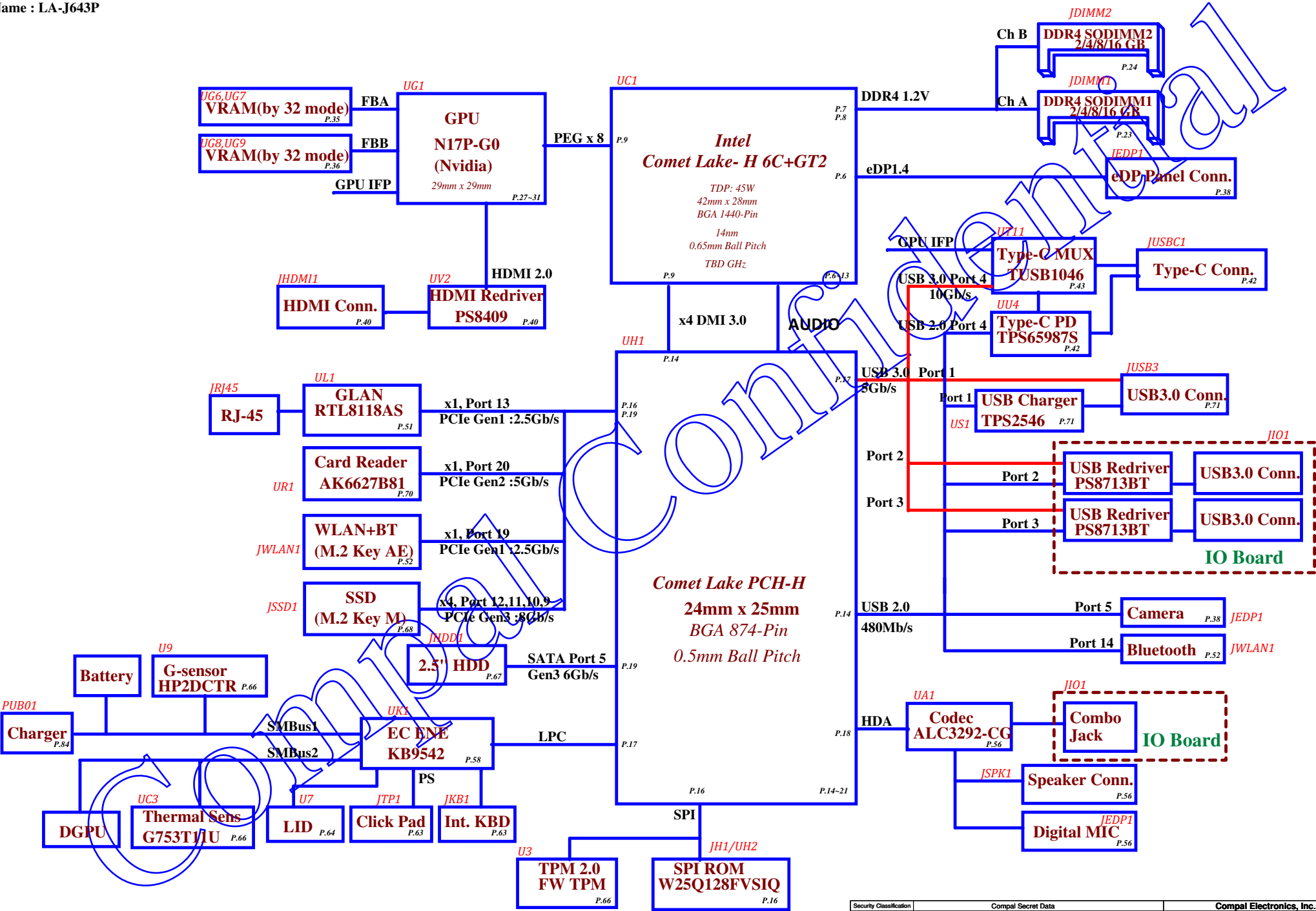
GPC52 MB Schematic Document

LA-J643P

Version 1.0

Date : 2020/03/13

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Issued Date	2017/07/24	Deciphered Date	2018/08/24	Title	
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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID / PCB Revision	Rb	Vad_BID_min	Vad_BID_TYP	Vad_BID_Max	ECAD3
0 -> 0.1	0		0V	0.300 V	0x00 - 0x13
1 -> 0.2	12K +/- 1%	0.347 V	0.354 V	0.36 V	0x14 - 0x1E
2 -> 0.3	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3 -> 0.4	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4 -> 0.5	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5 -> 0.6	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6 -> 0.7	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7 -> 0.8	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8 -> 0.9	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9 -> 1.0	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10 -> 1.1	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11 -> 1.2	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12 -> 1.3	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13 -> 1.4	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14 -> 1.5	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15 -> 1.6	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16 -> 1.7	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17 -> 1.8	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18 -> 1.9	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19 -> 2.0	NC	3.000 V	3.000 V	3.000 V	0xF1 - 0xFF

HSIO Port Table(CPU)

HSIO Port	Device	PCIE CLK&CLKREQ	HPD
PEG	DGPU (DIS)	CLK4 & CLKREQ#4	
DDI1	TYPE-C PORT		DDPB_HPDD0
DDI2	---		DDPC_HPDD1
DDI3	---		
eDP	embedded Display		EDP_HPDD

Power State

STATE \ SIGNAL	SLP_#3#	SLP_#4#	SLP_#5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCH SMBUS Address Table

PCH_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
PCH_SMBCLK PCH_SMBDATA	+3V_PCH_PRIM	JDIMM1	0X50	0XA0	0XA1
		JDIMM3	0X52	0XA4	0XA5
		TOUCH PAD			
PCH_SML0CLK PCH_SML0DATA	+3V_PCH_PRIM	NA			
PCH_SML1CLK PCH_SML1DATA	+3V_PCH_PRIM	EC	TBC	TBC	TBC
		GPU	0x41		

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SMBUS Port1	+3V _{SMBUS}	BAT	0x16	TBC	TBC
		CNCR	0x09	0x12	0x13
		G-Sensor	0x29	0x52	0x53
		PCD	TBC		
SMBUS Port2	+3V _L	GPU	0x41		
		THERMAL	0x48	0X90	0x91
		PD	0x3F	0X71	0x70
		Type-C MUX	0x10	0X20	0x21
			0x11	0X22	0x23

I2C Address Table

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
I2C_0_SCL I2C_0_SDA	+3VS				
I2C_1_SCL I2C_1_SDA	+3VS				

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	D53
VIN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF
+VCC_SA	System Agent voltage Supply	ON	OFF	OFF	OFF	OFF
+VCC_GT/+VCC_GTX	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+VCC_EOPIO/+VCC_EDRAM	Processor EOPIO/EDRAM supply	ON	OFF	OFF	OFF	OFF
+1.05VALW	System +1.0V power rail	ON	ON	ON	ON*	OFF
+0.95VS_VCCIO	+1.0VS IO power rail	ON	ON	ON	OFF	OFF
+1.05V_VCCMPHY	+1.0V power for PCH MODPHY rails	ON/OFF	ON/OFF	ON/OFF	ON/OFF	OFF
+0.95VS_DGPU	+0.95VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	ON	OFF	ON
+1.5VS_MEM_GFX	+1.5VS power rail for GPU/VRAM	ON	OFF	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*	OFF
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+2.5V	DDR4 +2.5Vpp power rail	ON	ON	ON	OFF	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VALW	+3VALW power for PCH suspend rails	ON	ON	ON	ON*	ON
+3VALW_DSWS	+3VALW power for PCH PSW rails	ON	ON	ON	ON*	ON
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON	ON
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

BOM Structure Table (1/2)

Function	Stuff	Un-Stuff
CFL-H SKU	CFL_H@	
DGPU SKU	DIS@	
VRAM STRAP/3G	3G@	
VRAM STRAP/6G	6G@	
GC6	GC6@	@GC6@
Touch		TS@
eSPI I/F	I PC@	FSPI@
TPM 9665	9665@	@9665@
TPM 9670	9670@	@9670@
CNVI	CNVI@	@CNVI@
EMI Components	VGA@ EMI@	@EMI@
ESD Components	ESD@	@ESD@
RF Components	RF@	@RF@
XDP	XDP@	
ME Connector	CONN@	
STANDOFF	STD@	
For Signal Test	MP@	
VGA POWER SKU	VGA@	

HSIO Port Table(PCH)

HSIO Port	Capable	USB3.0	PCIe	SATA	Device	PCIe CLK&CLKREQ	NOTE
0	USB3.1_1(OTG)	1			USB3.1 PORT 1		
1	USB3.1_2 /	2			USB3.1 PORT 2		
2	USB3.1_3	3			USB3.1 PORT 3		
3	USB3.1_4	4			TYPE-C PORT		
4	USB3.1_5	5					
5	USB3.1_6	6					
6	USB3.1_7 / PCIe_1	7	1				
7	USB3.1_8 / PCIe_2	8	2				
8	USB3.1_9 / PCIe_3	9	3				
9	USB3.1_10 / PCIe_4	10	4				
10	PCIe_5 / GbE		5				
11	PCIe_6		6				
12	PCIe_7		7				
13	PCIe_8		8				
14	PCIe_9 / GbE		9				
15	PCIe_10		10				
16	PCIe_11 / SATA_0A		11	0	NGFF SSD Optane memory SSD	CLK2 & CLKREQ#2	Support SATA function on SATA#1
17	PCIe_12 / GbE / SATA_1A		12	1			
18	PCIe_13 / GbE / SATA_0B		13	0	LAN	CLK5 & CLKREQ#5	
19	PCIe_14 / SATA_1B		14	1			
20	PCIe_15 / SATA_2		15	2			
21	PCIe_16 / SATA_3		16	3			
22	PCIe_17 / SATA_4		17	4			
23	PCIe_18 / SATA_5		18	5	HDD		
24	PCIe_19		19		WLAN	CLK1 & CLKREQ#1	
25	PCIe_20		20		CARD READER	CLK3 & CLKREQ#3	
26	PCIe_21		21				
27	PCIe_22		22				
28	PCIe_23		23				
29	PCIe_24		24				

USB2.0 Port Table

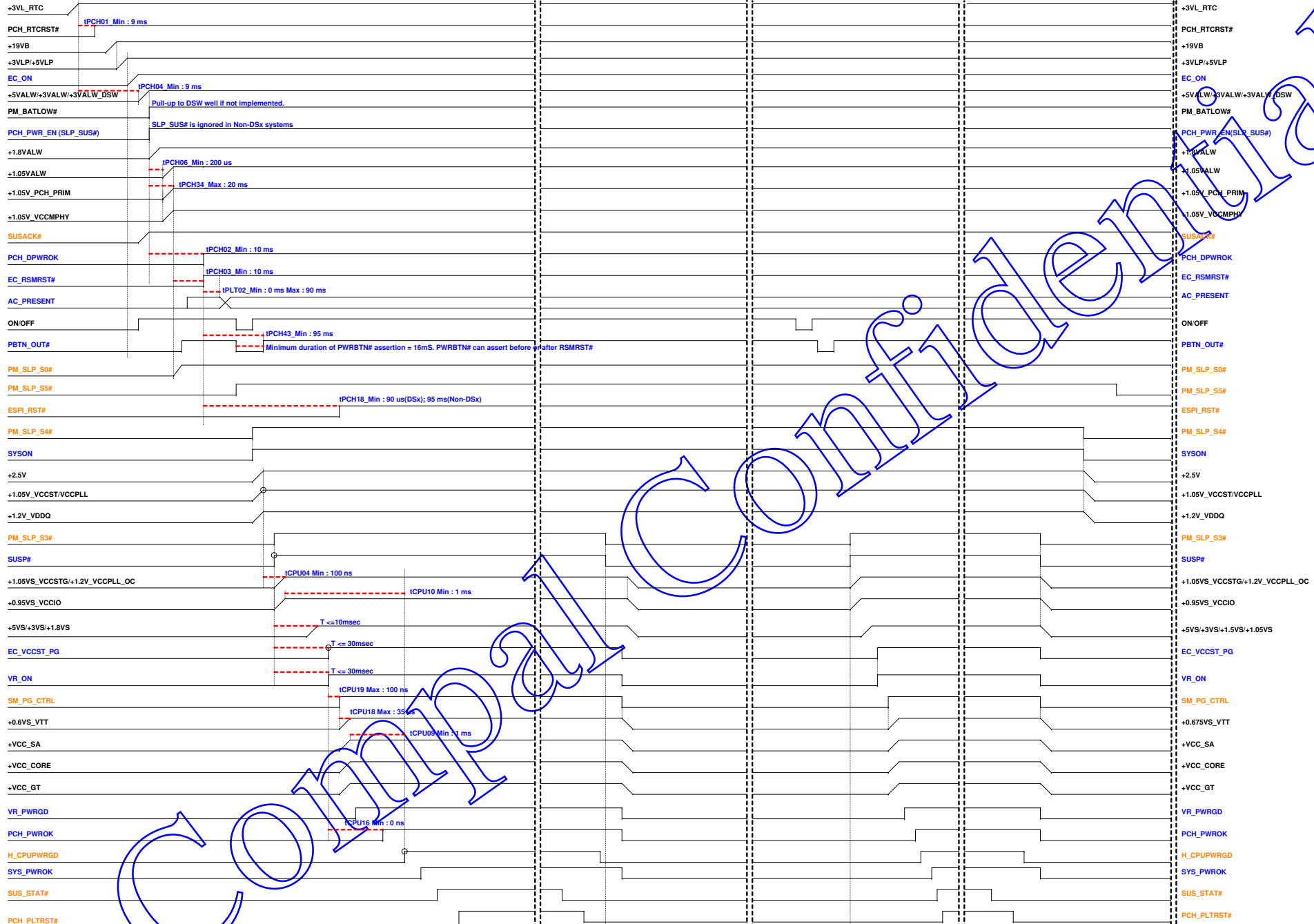
USB2	Function
1	USB3.1 PORT 1
2	USB3.1 PORT 2
3	USB3.1 PORT 3
4	TYPE-C PORT
5	IR Camera
6	
7	Touch Panel
8	
9	
10	
11	
12	
13	
14	WLAN+BT Module

G3→S0

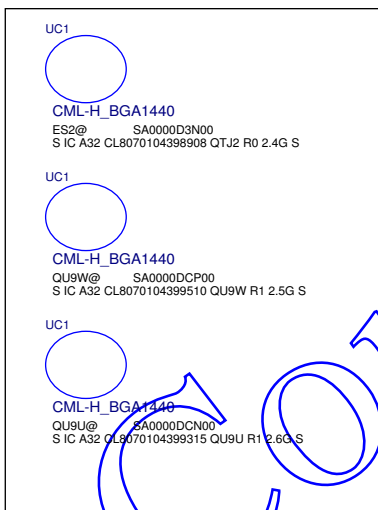
S0→S3

S3→S0

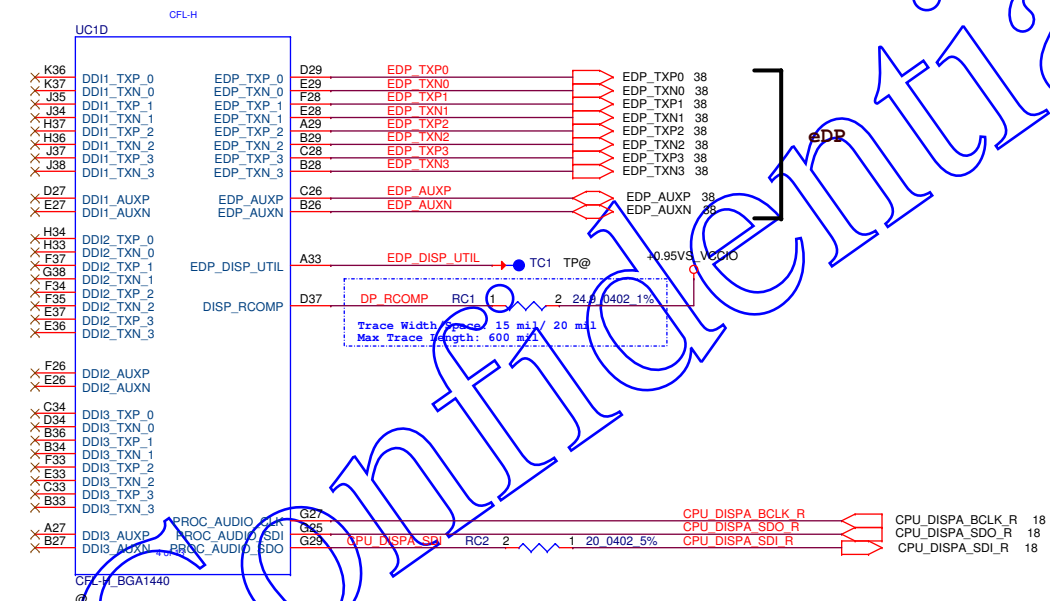
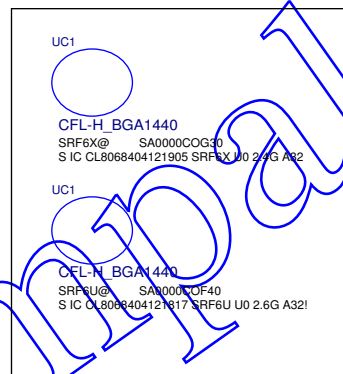
S0→S5



Comet Lake-H CPU SKU



R3



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CHANNEL-A

Interleaved Memory



CHANNEL-B

Interleaved Memory



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To DGPU
PEG Lane Reversed

To DGPU
PEG Lane Reversed

+0.95VS_VCCIO

RC9 1 2 24.9 0402 1%

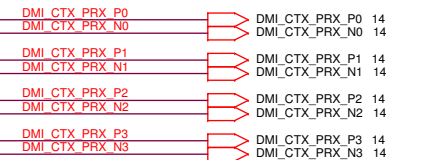
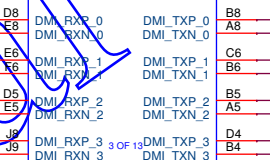
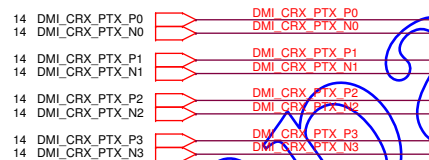
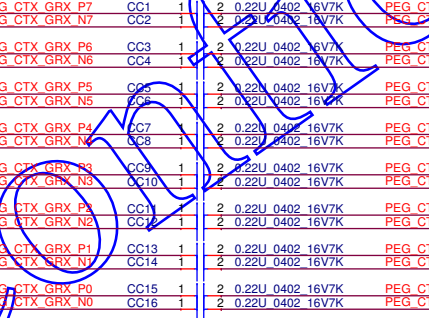
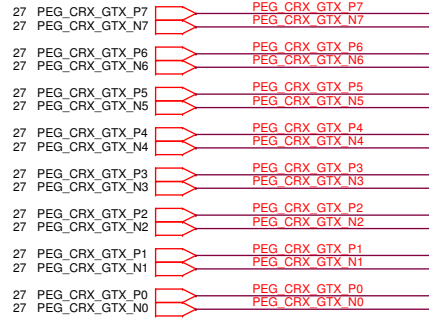
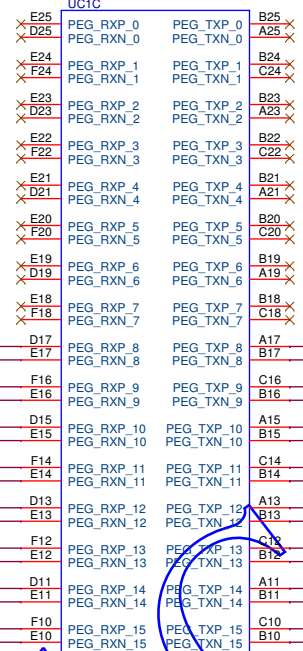
PEG RCOMP

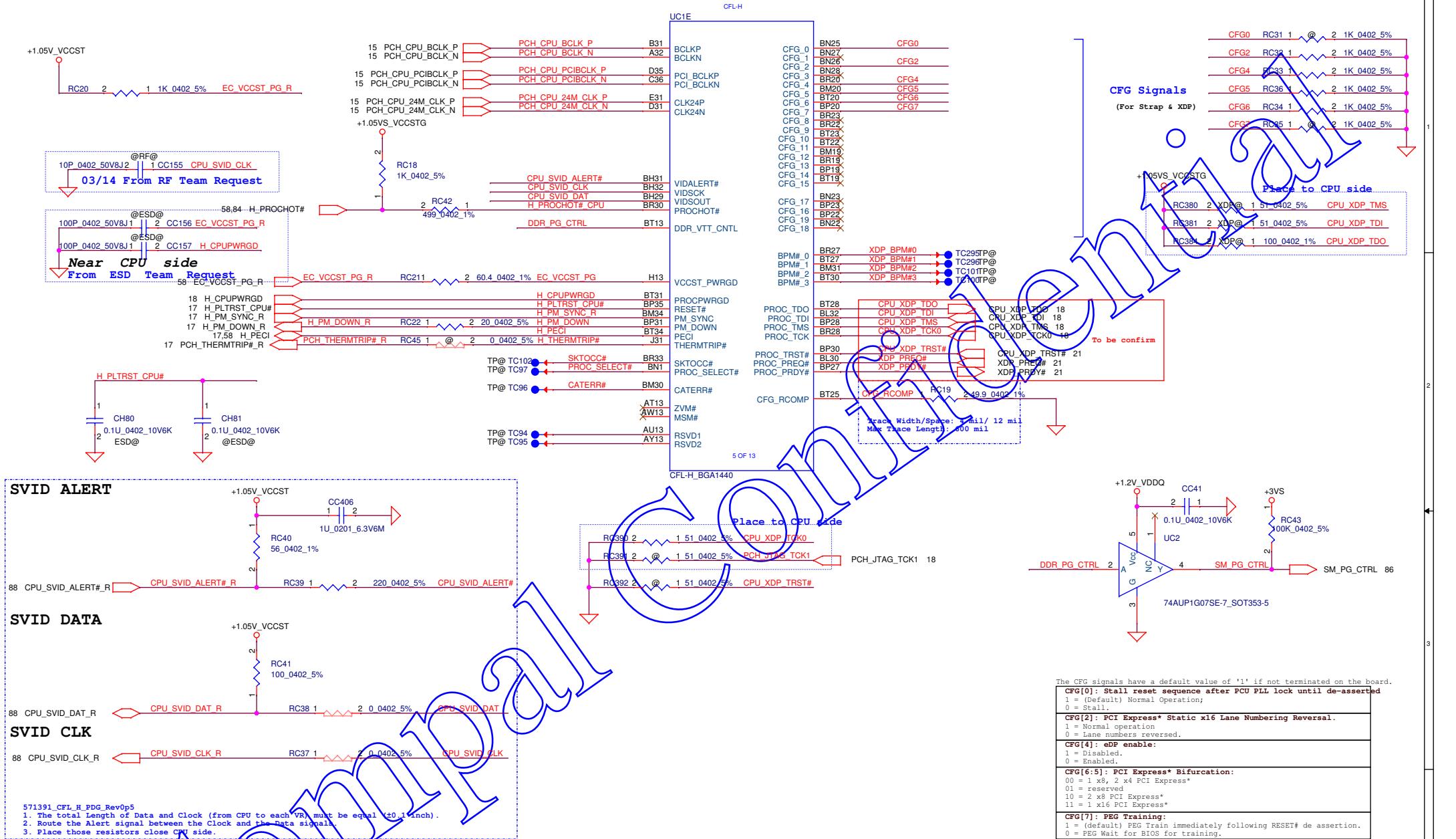
Trace Width/Space: 15 mil/ 15 mil
Max Trace Length: 600 mil

To PCH

To PCH

UC1C
CFL-H
CFL-H_BGA1440
@





SVID ALERT

88 CPU_SVID_ALERT#_R CPU_SVID_ALERT# R

SVID DATA

88 CPU_SVID_DAT_R CPU_SVID_DAT R

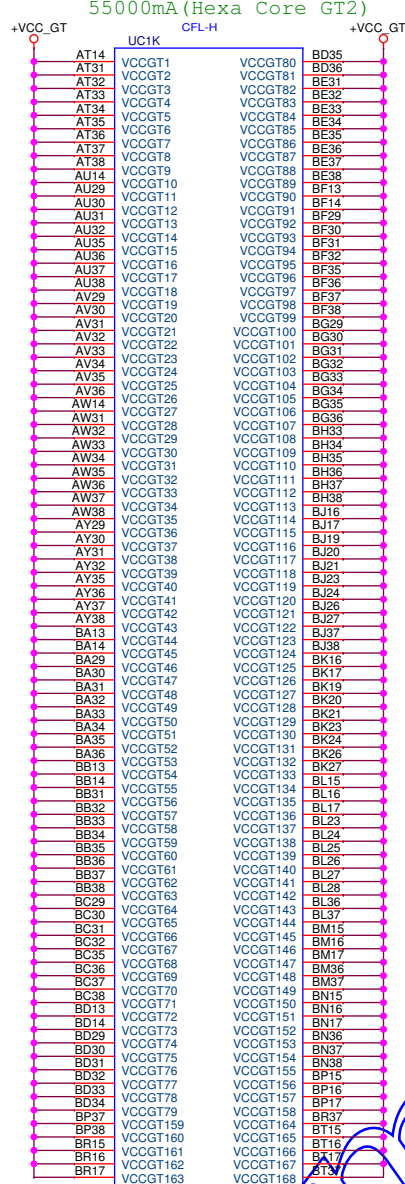
SVID CLK

88 CPU_SVID_CLK_R CPU_SVID_CLK R

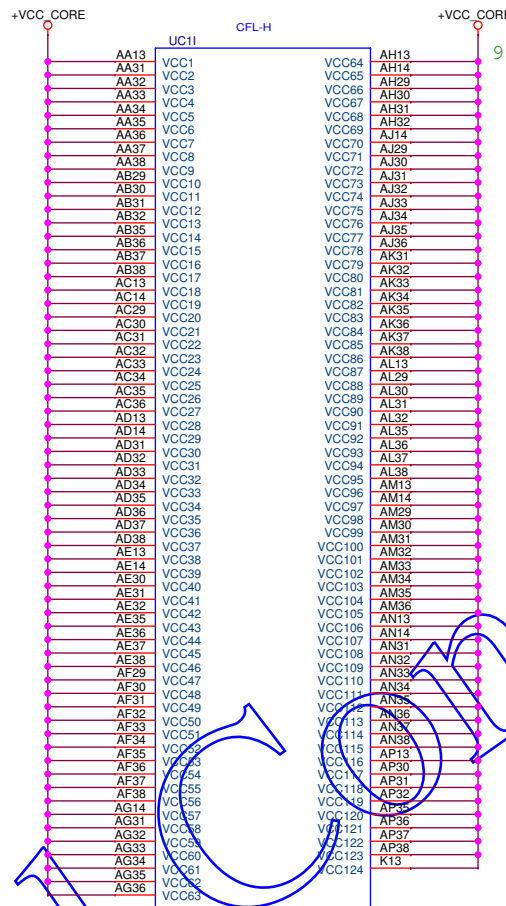
571391_CFL_H_PDG_Rev0p5

1. The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
2. Route the Alert signal between the Clock and the Data signals.
3. Place those resistors close CPU side.

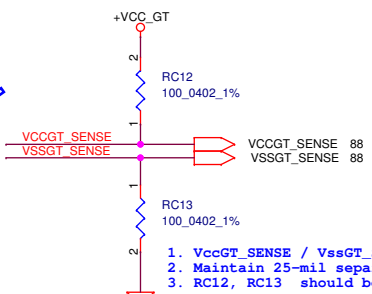
GT
55000mA (Hexa Core GT2)



11 OF 13 VCCGT_SENSE
VSSGT_SENSE
VCCGT_SENSE

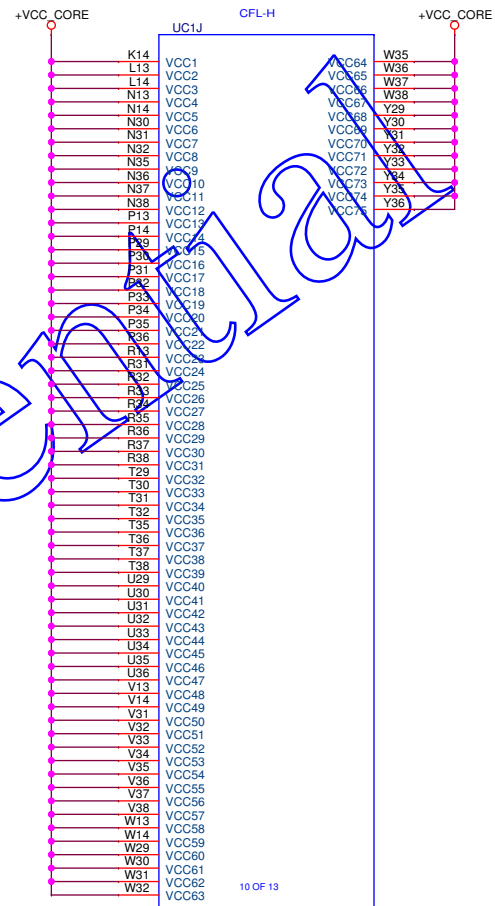


9 OF 13 VCC_SENSE
VSS_SENSE

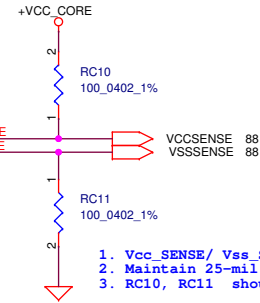


1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC12, RC13 should be placed within 2 inches (50.8 mm) of CPU

96000mA (Hexa Core GT2)

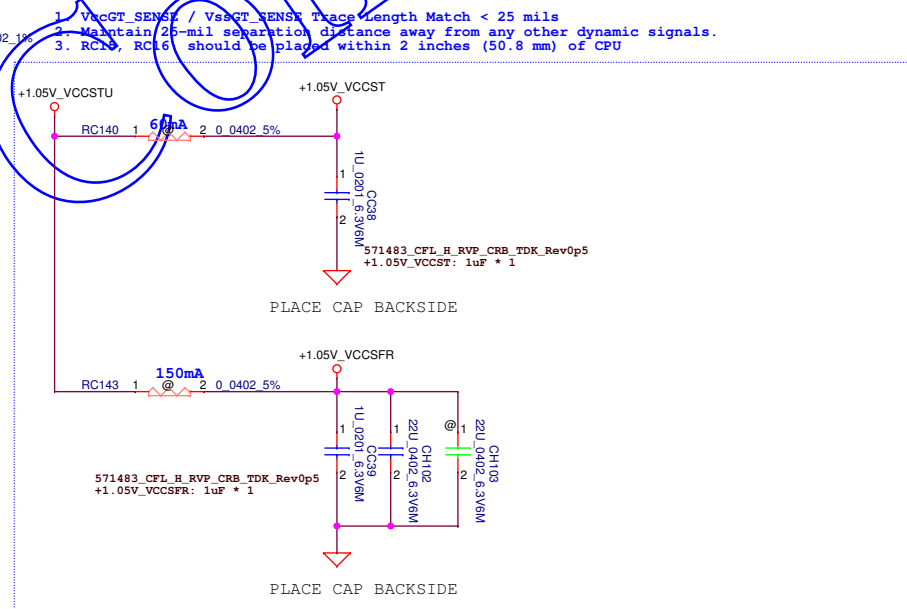
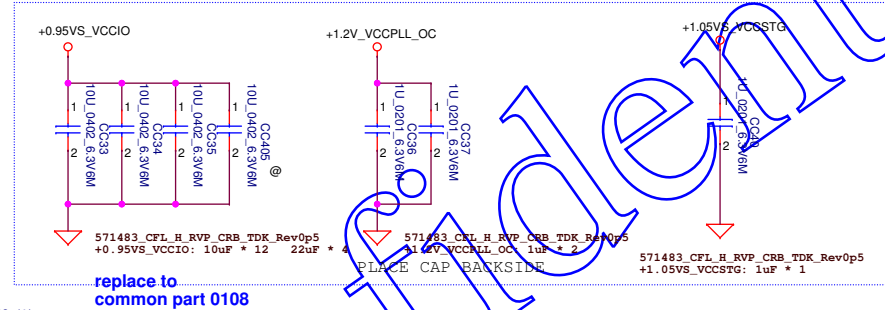
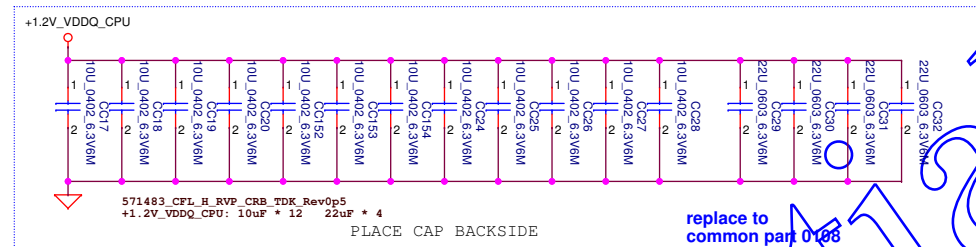
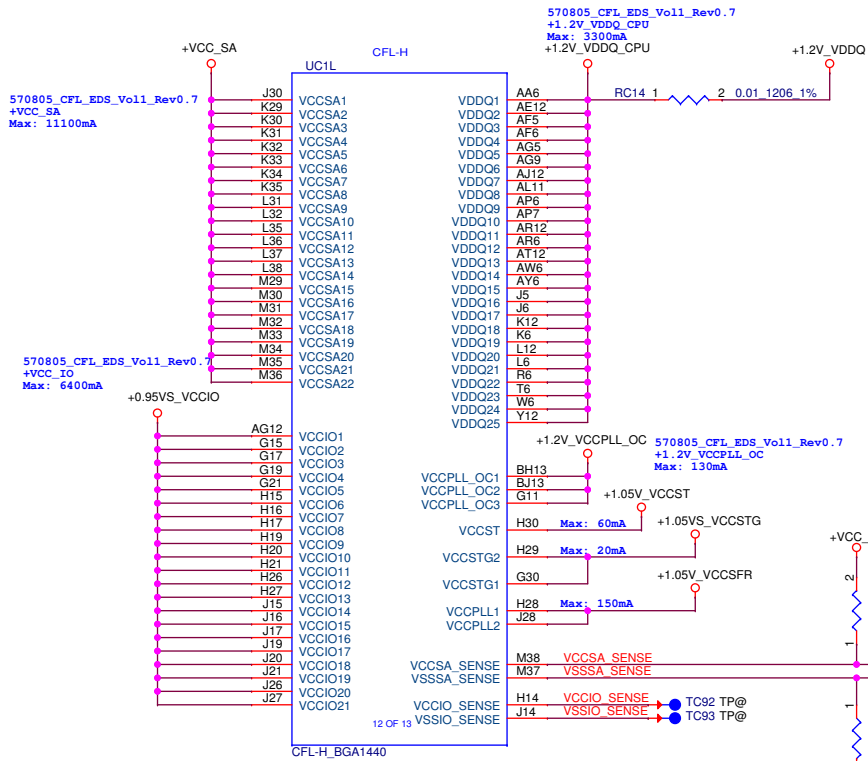


10 OF 13 CFL-H_BGA1440

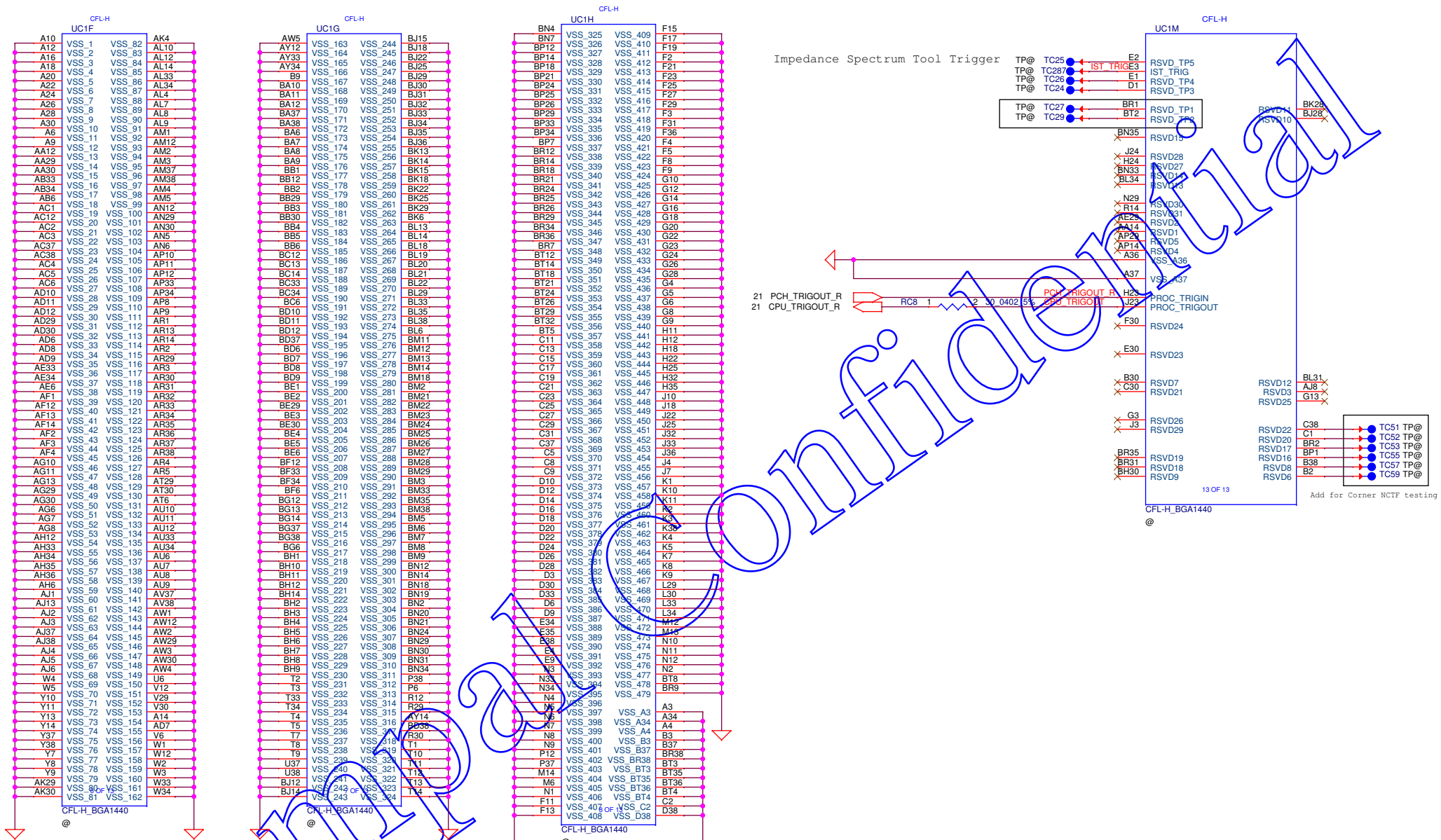


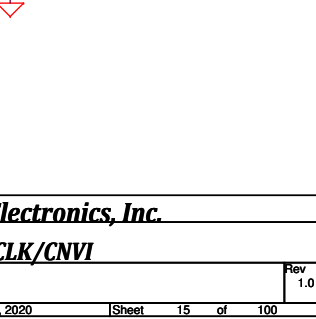
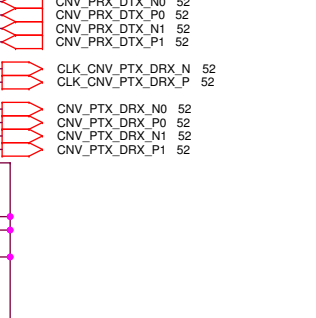
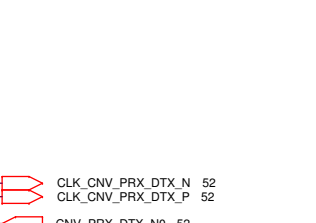
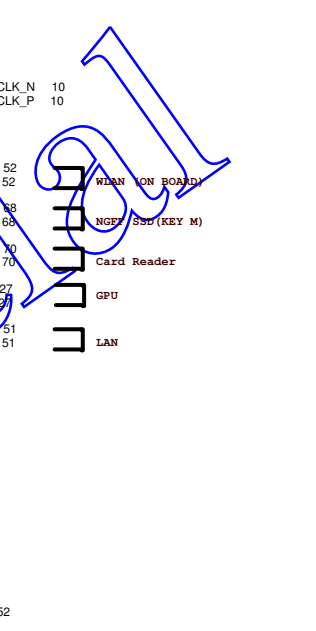
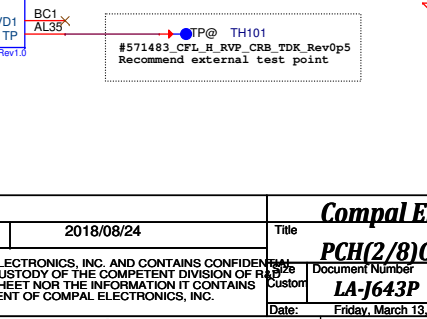
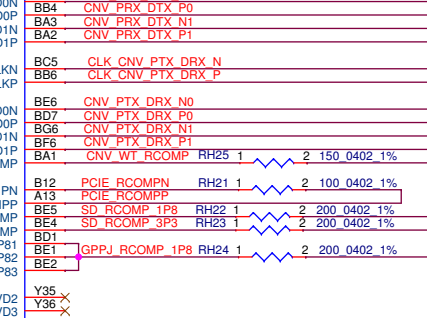
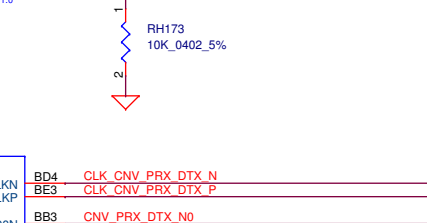
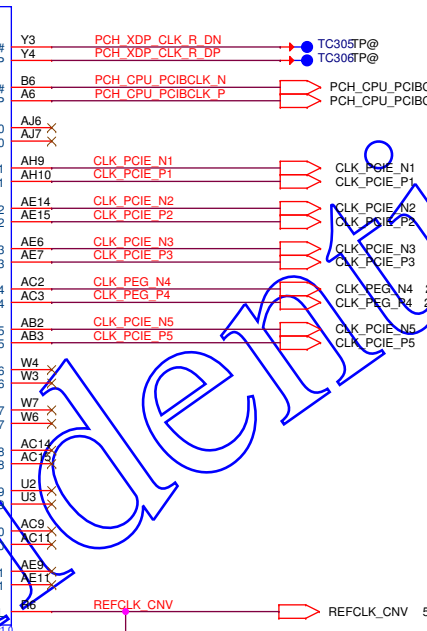
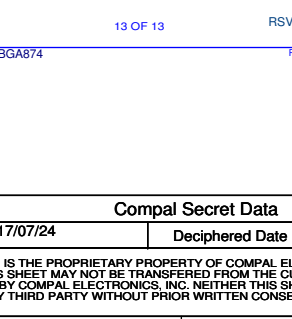
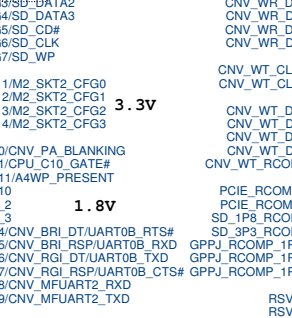
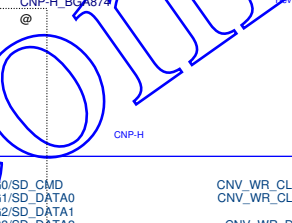
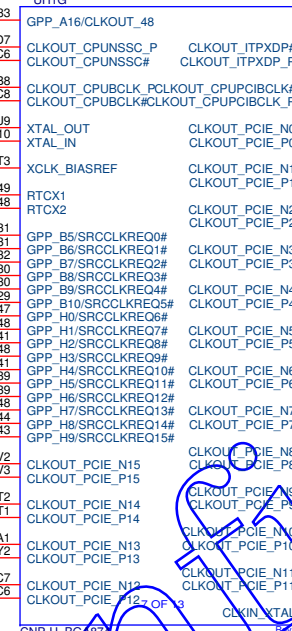
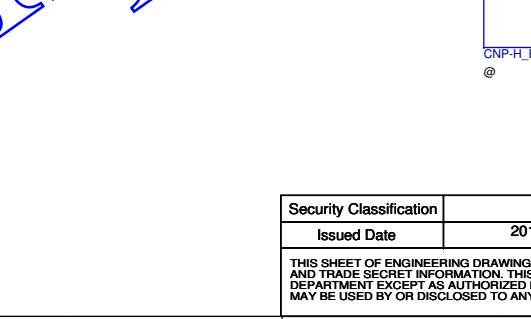
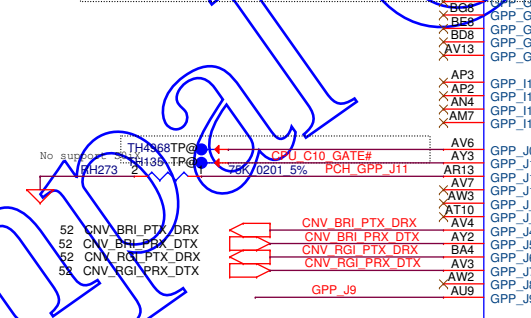
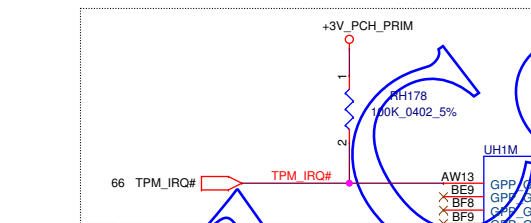
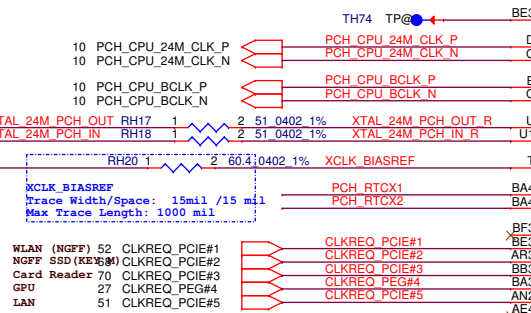
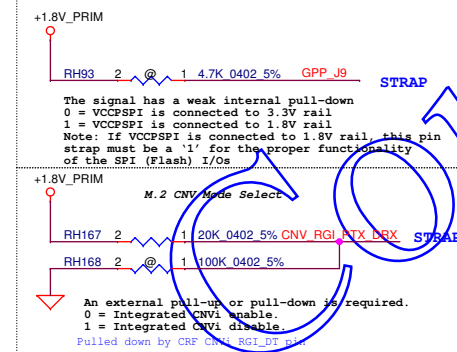
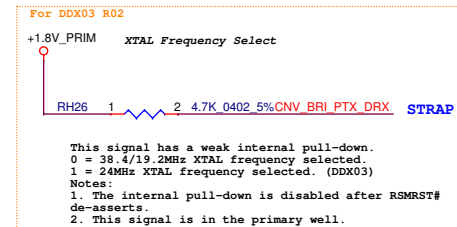
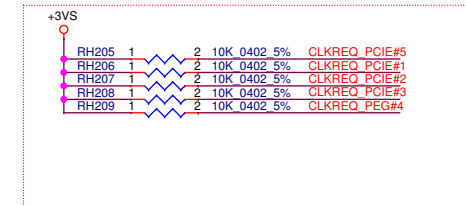
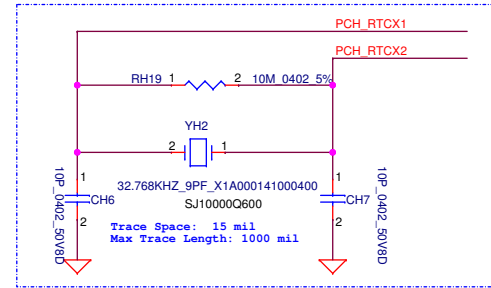
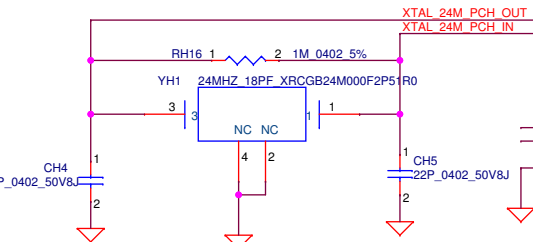
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								Date:		Friday, March 13, 2020		Sheet		11 of 100	
								C		D		E		F	

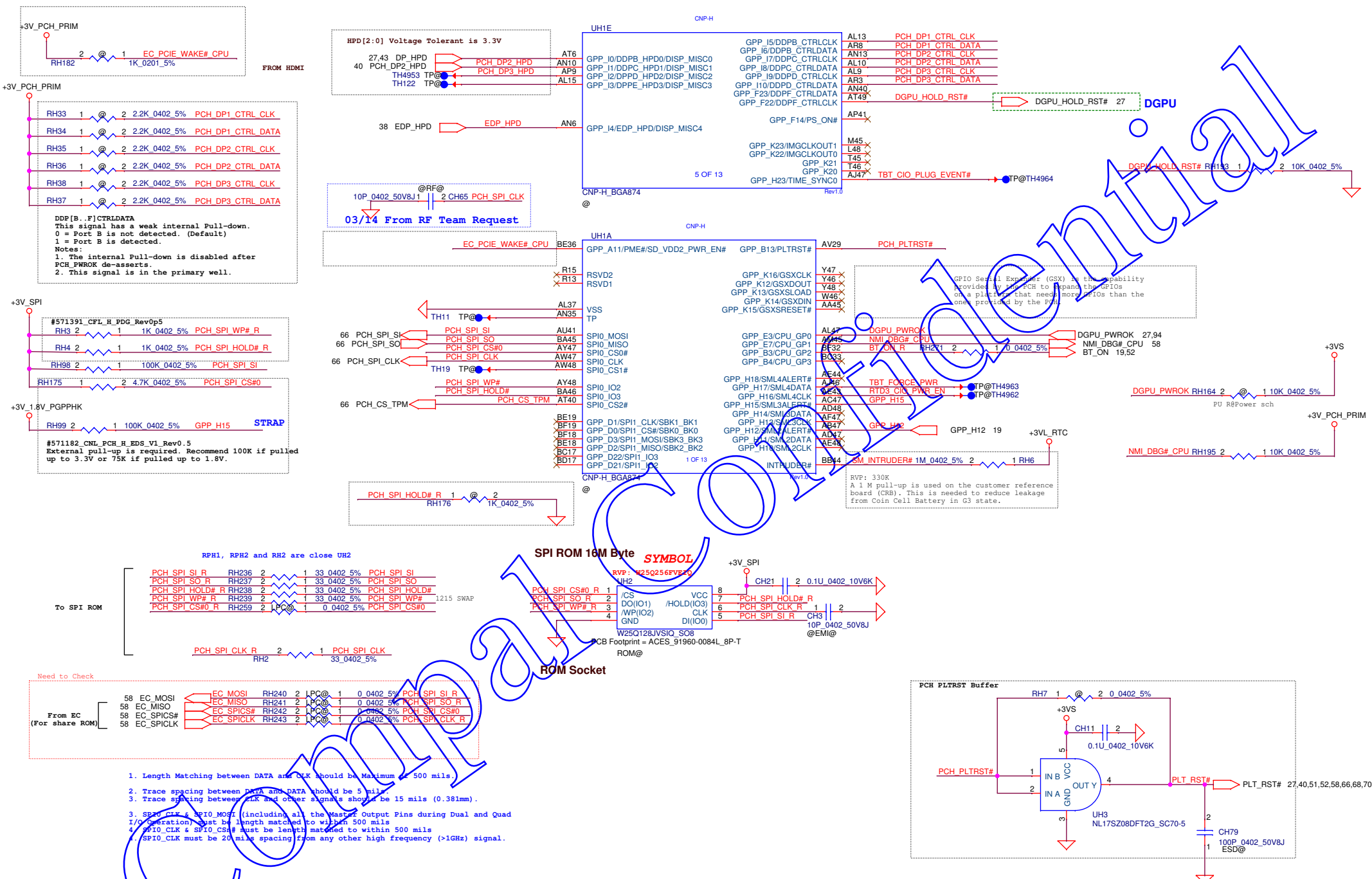


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				Sheet	12 of 100

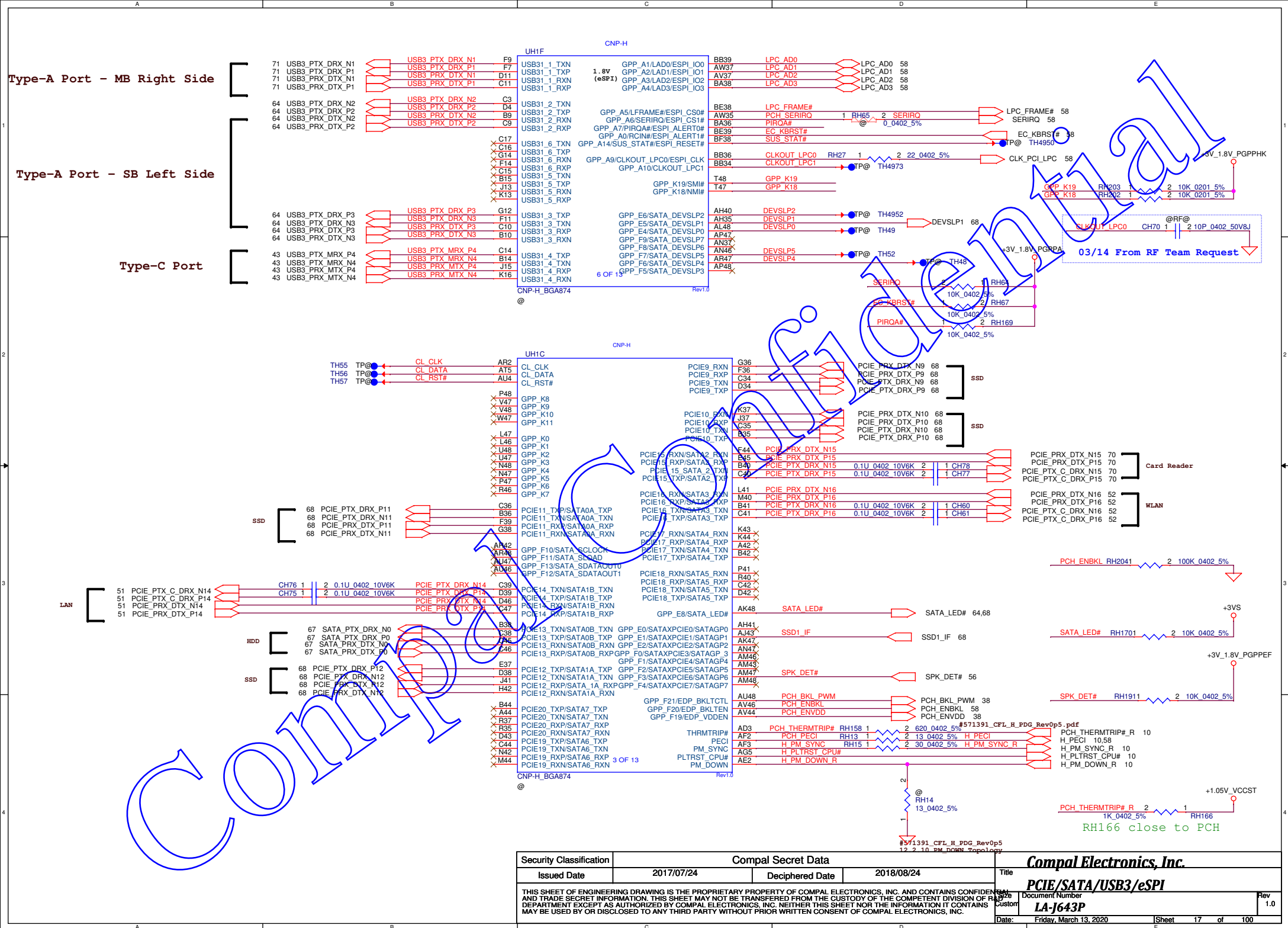


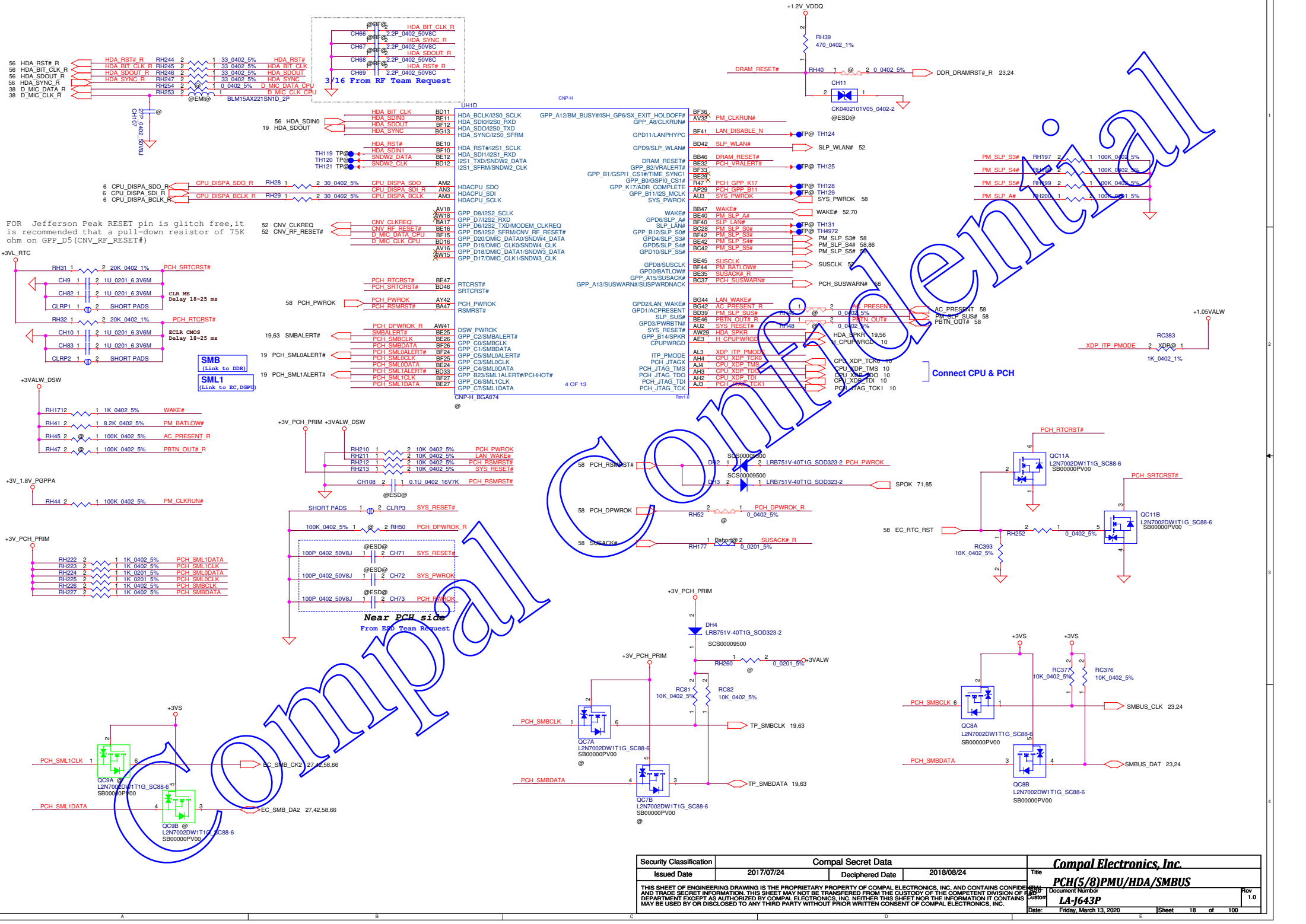


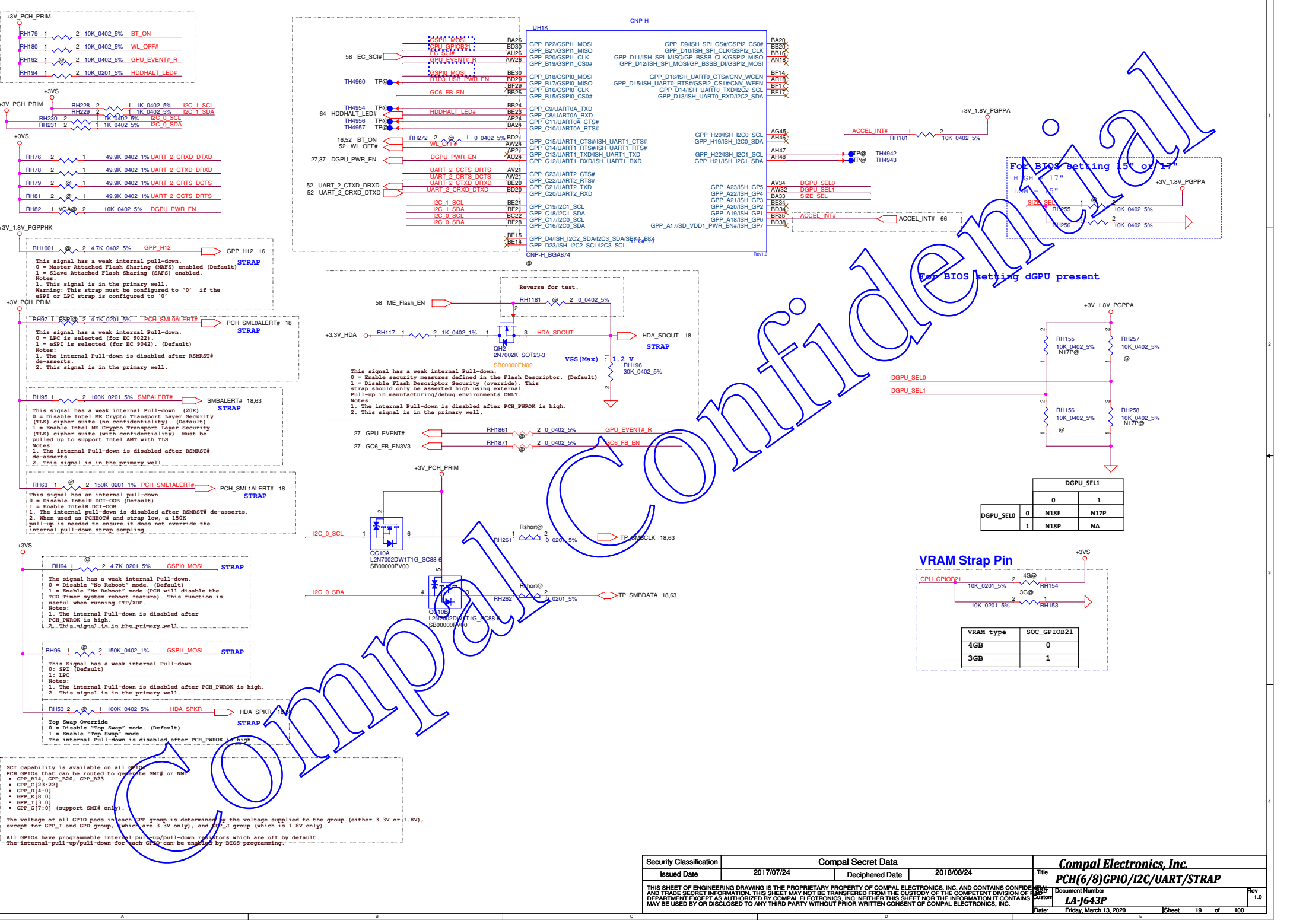
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For BIOS setting 15" or 17"

HIGH 1.7"

LOW 1.5"

SIZE SEL

RH255 10K_0402_5%

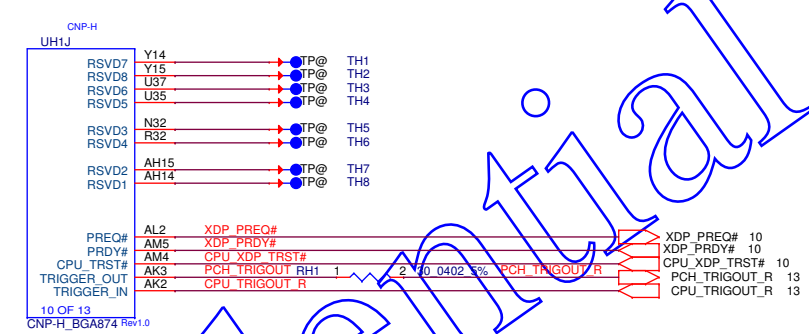
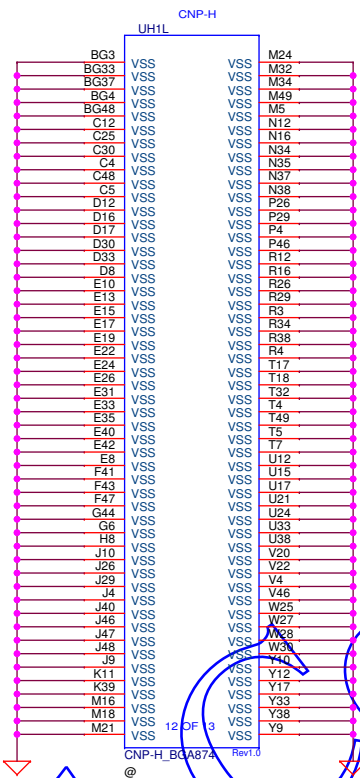
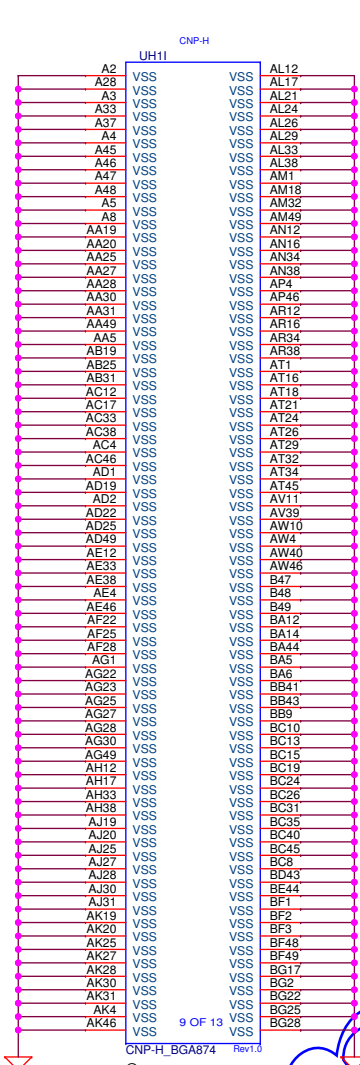
RH256 10K_0402_5%

DGPU_SEL1		
	0	1
DGPU_SEL0	N18E	N17P
	N18P	NA

VRAM Strap Pin	
CPU_GPIOB21	10K_0201_5%
	4G@ 1
	3G@ 1
	10K_0201_5%

VRAM type	SOC_GPIOB21
4GB	0
3GB	1

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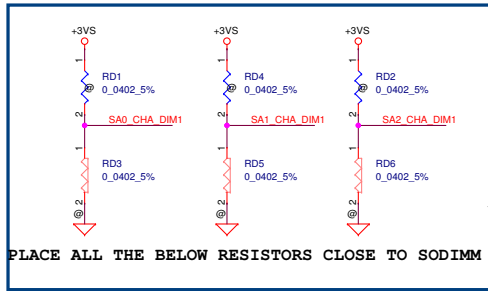
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CHANNEL-A

TOP REVERSE TYPE (4 mm)

Interleaved Memory

TOP: JDIMM1 CONN Non-ECC DIMM

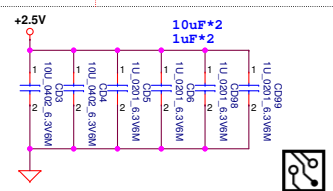


PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

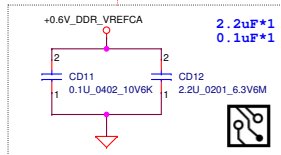
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM1.257,259

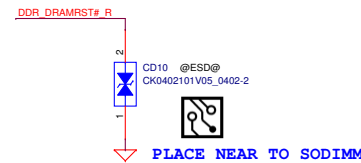
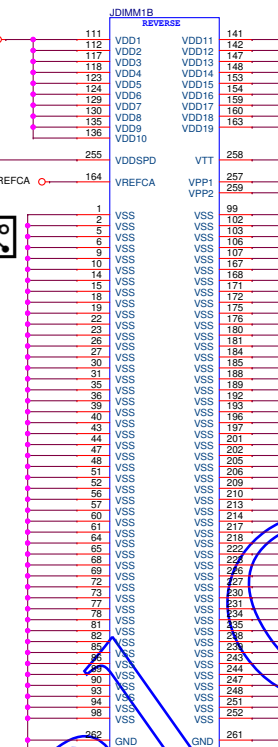
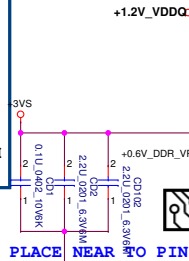
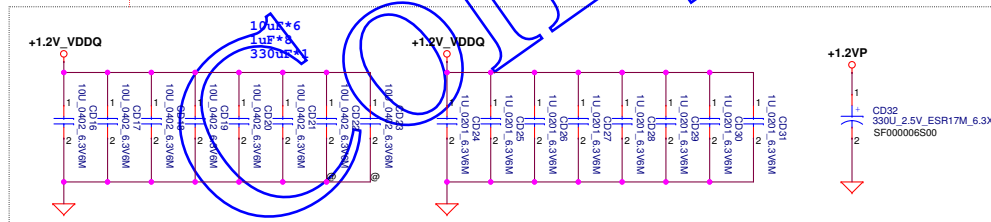
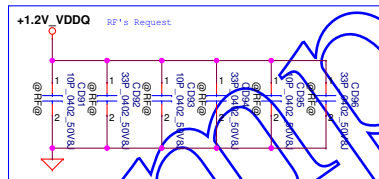
Layout Note:
Place near JDIMM1.258



Layout Note:
PLACE THE CAP near JDIMM1. 164



Layout Note:
Place near JDIMM1



+1.2V_VDDQ

DIMM Side

CPU Side

VREF traces should be at least 20 mils
wide with 20 mils spacing to other
signals

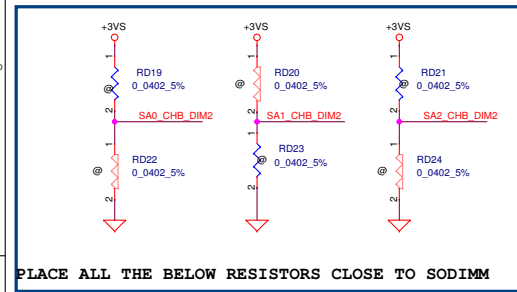
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		DDRIV_CHA: DIMM0
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CHANNEL-B

TOP STD (4 mm)

Interleaved Memory

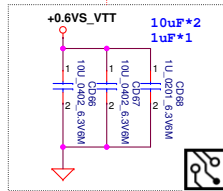
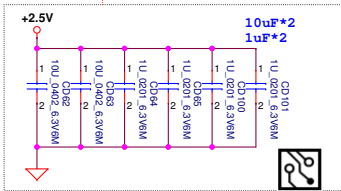
TOP: JDIMM2 CONN Non-ECC DIMM



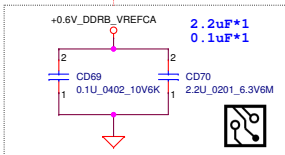
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM2.257,259

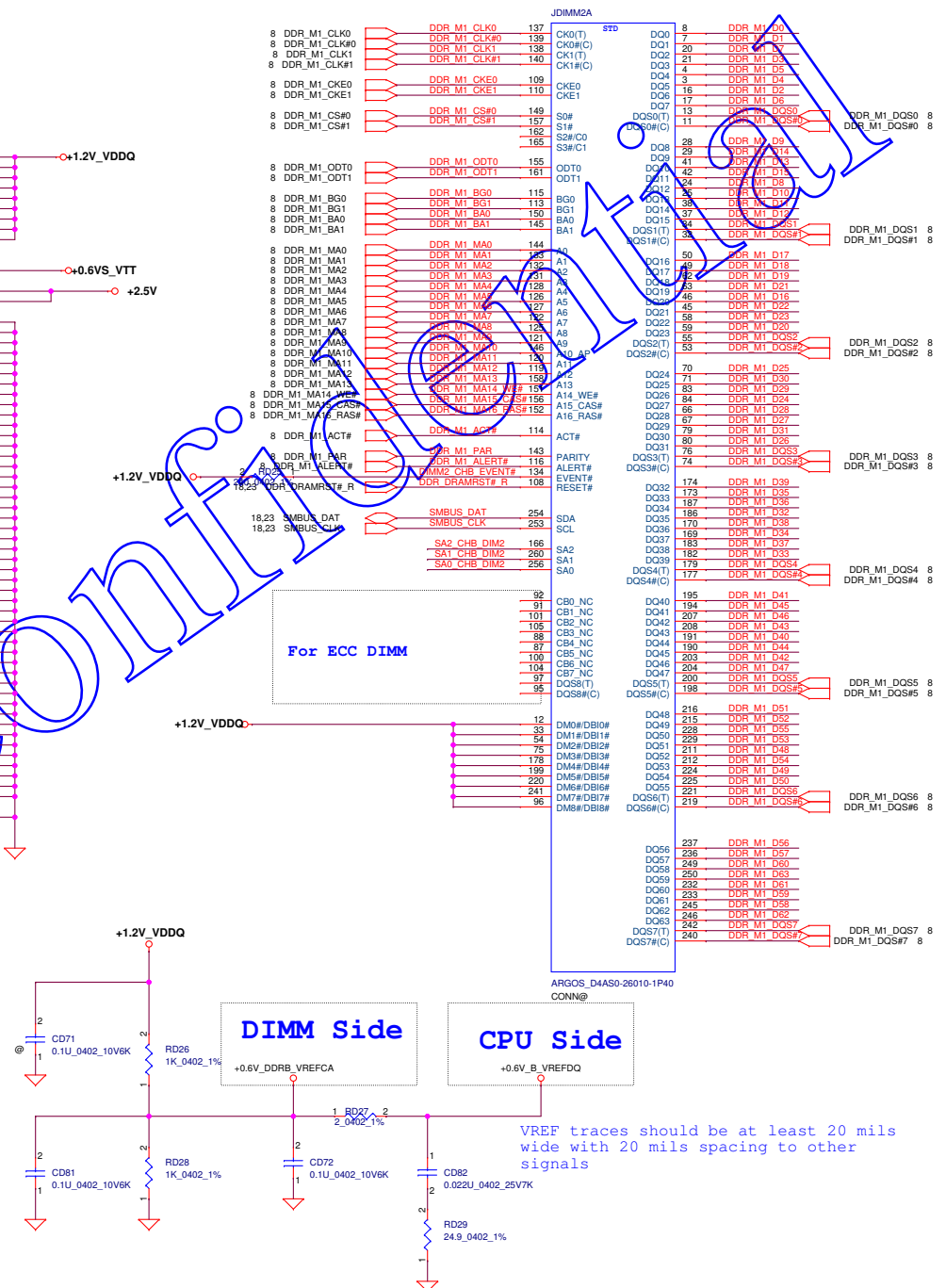
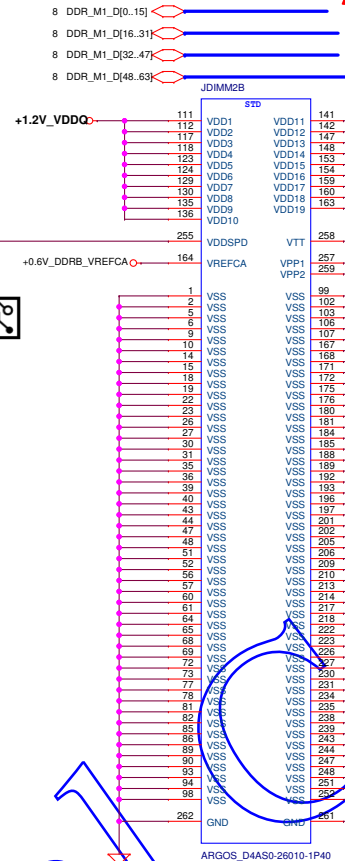
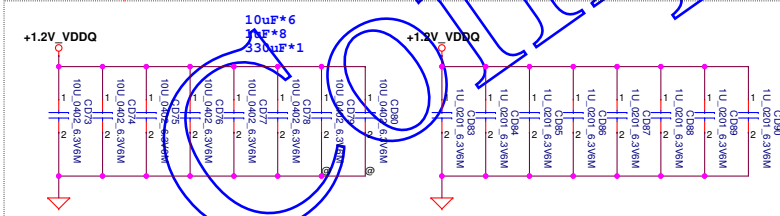
Layout Note:
Place near JDIMM2.258



Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM2



Layout Note:
Place near JDIMM2



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				LA-1643P		
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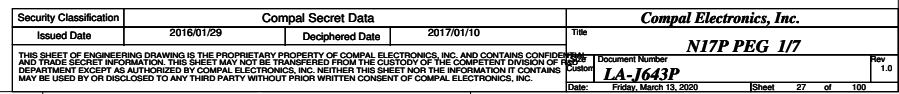
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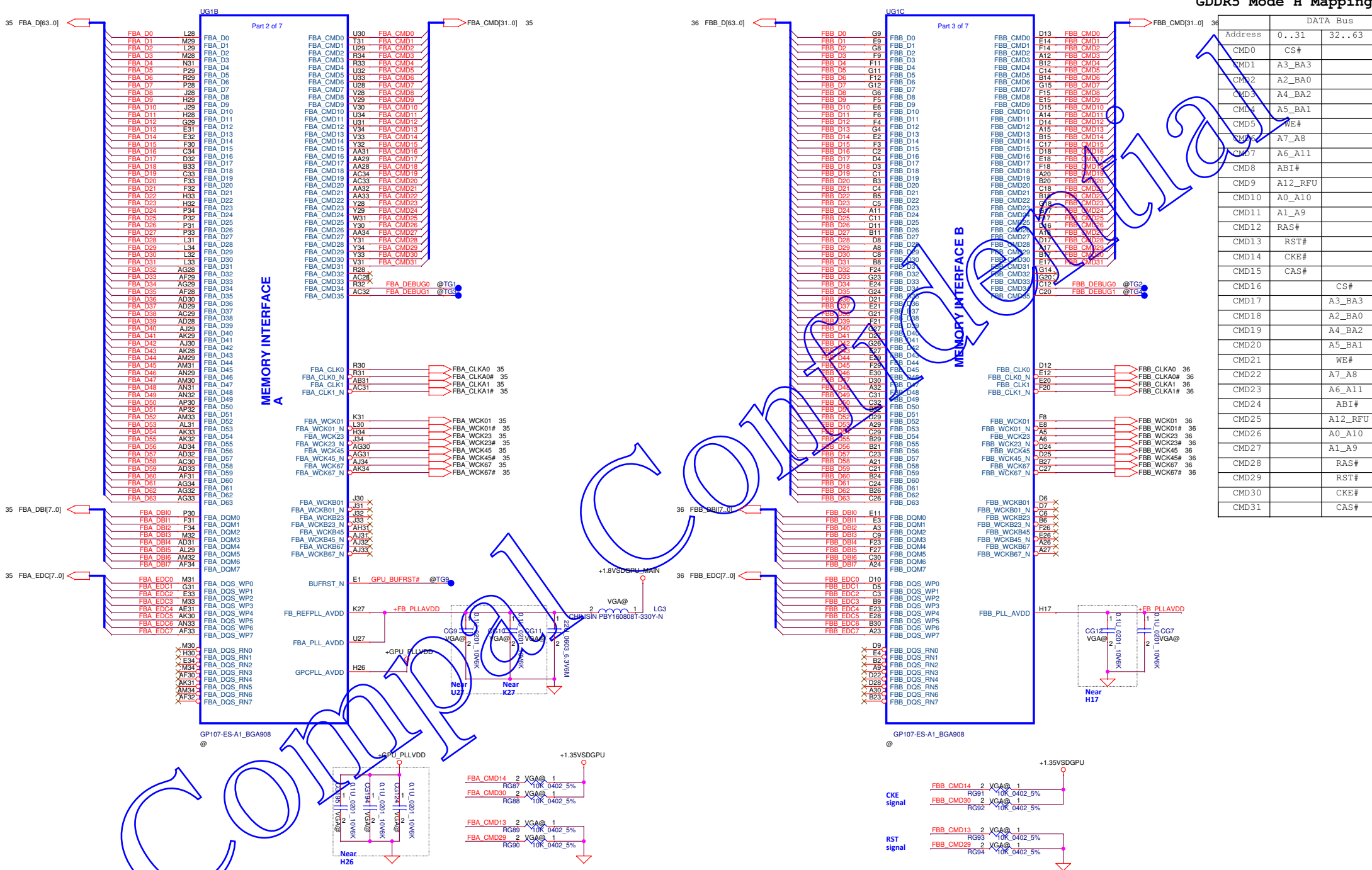
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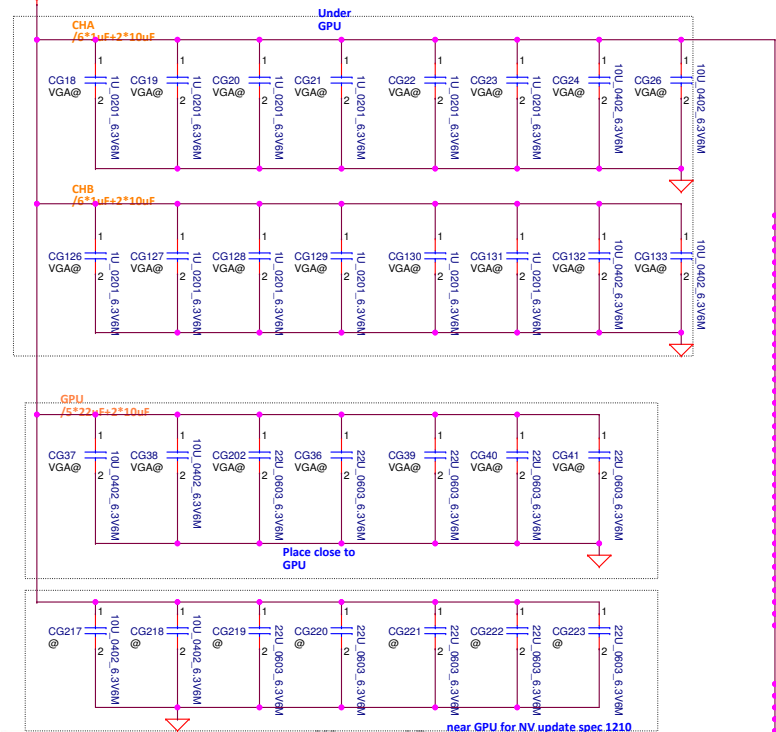
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GDDR5 Mode H Mapping



+1.35VSDGPU

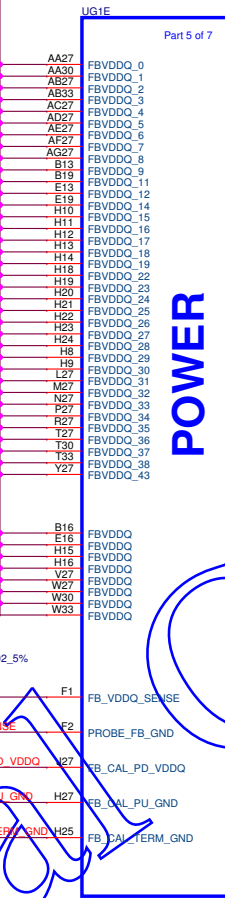


Memory	FBVDDQ	FB_CAL_PU_GND	FB_CAL_PD_VDDQ	FB_CAL_TERM_GND
GDOR5	1.5 V	40.2 Ω	40.2 Ω	60.4 Ω
	1.55 V			
GDOR5	1.35 V	40.2 Ω	40.2 Ω	60.4 Ω

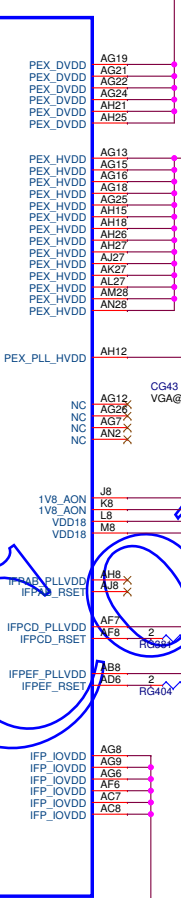
For N17x GPU Package: GB4C-128 (preliminary)				
Capacitor Type	Value	Footprint	Population	Location
1.0 uF	X65 [0402]	12	2	Under GPU FBVDDQ ball
10 uF	X65 [0603]	4	1	Near GPU device
10 uF	X65 [0603]	2	2	Near GPU device
22 uF	X65 [0603]	5	1	Near GPU device

GPU	Type	Footprint	Population	Location
N16P: IFPC, D, E, F, PLLVDD or N16E: IFPC, F, PLLVDD Supply Rails				
GB4B-128, GB4C-128	0.1 uF X7R 0402	3	2	N16P: Under GPU, 1 per ball
	1.0 uF X65 0402	2	1	N16E: Under GPU, 1 per ball
	4.7 uF X5R 0603	1	0	Near GPU
Bead Type				
	L2=300 Ω @ 100 MHz (ESR=0.25 Ω)	0603	1	Near GPU

GPU	Type	Footprint	Population	Location
IFPY_IOVDD (N17 IFP_IOVDD) Supply Rails				
GB4B-128, GB4C-128	0.1 uF X7R 0402	6	6	Under GPU, 1 per ball
	1.0 uF X65 0402	2	3	Near GPU
	4.7 uF X65 0603	2	3	Near GPU
Bead Type				
	L1=180 Ω @ 100 MHz (ESR=0.2 Ω)	0603	2	Near GPU



POWER



1*22uF+1*10uF+2*4.7uF+4*1uF

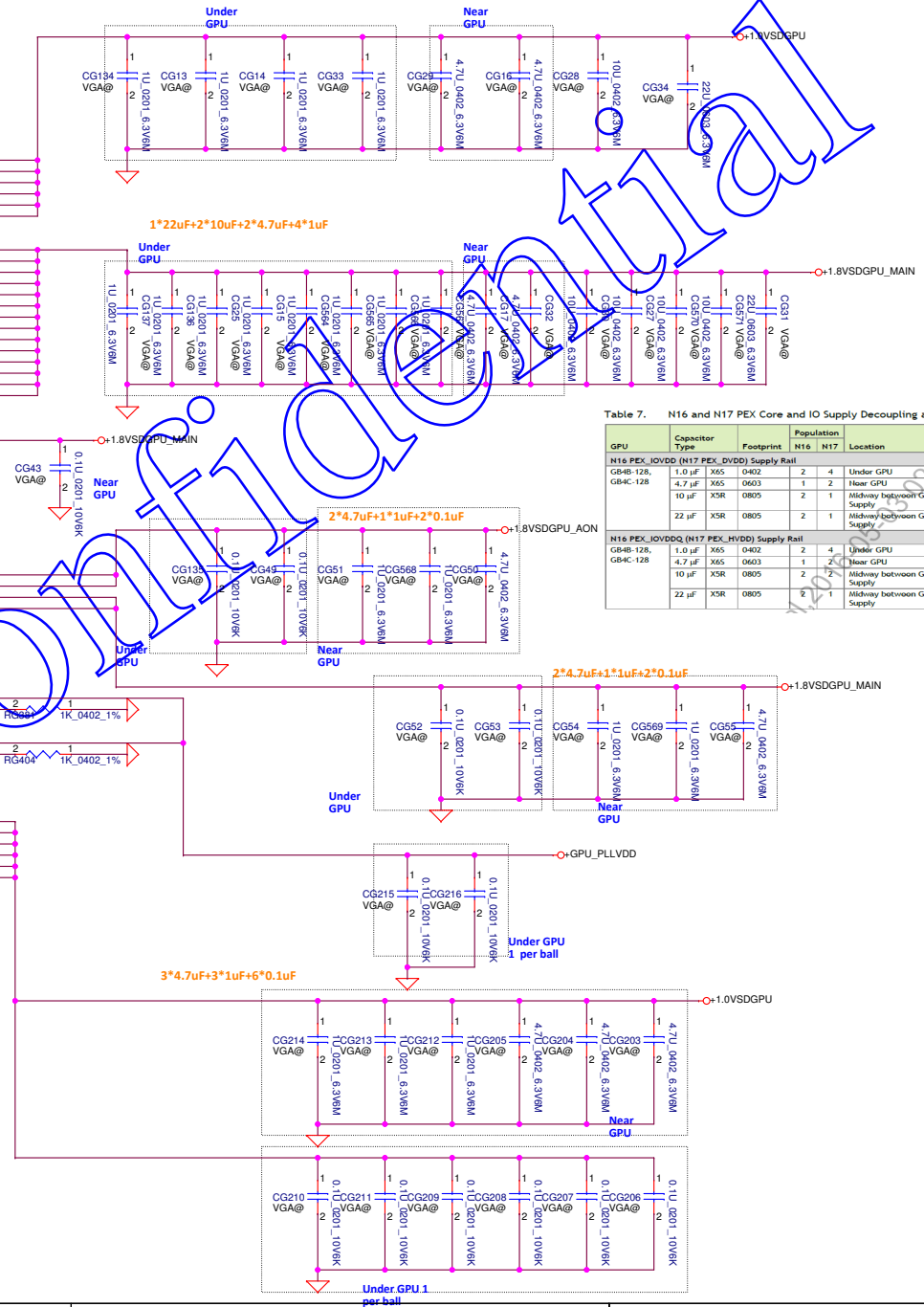
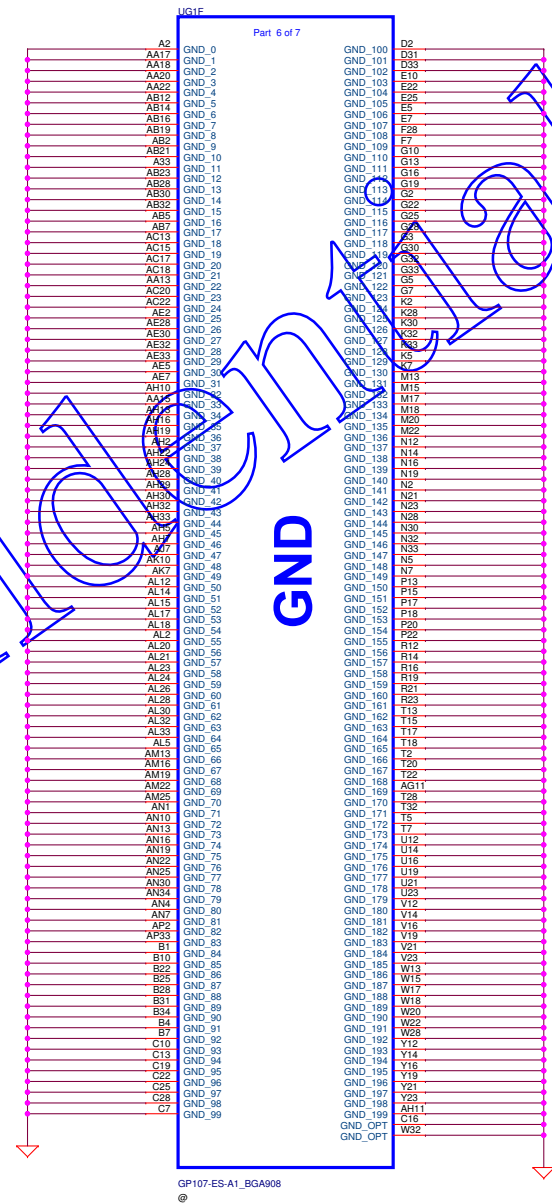
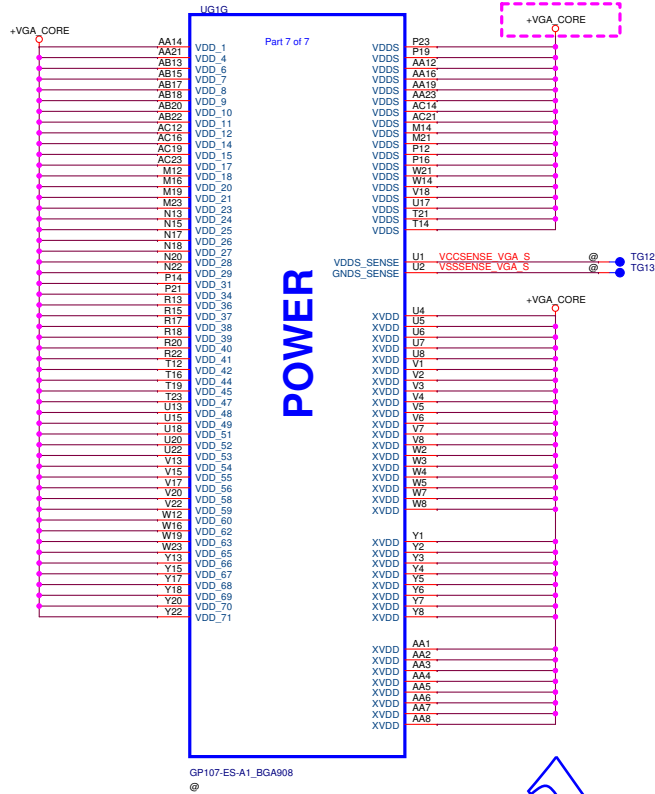


Table 7. N16 and N17 PEX Core and IO Supply Decoupling and Filtering				
GPU	Capacitor Type	Footprint	Population	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail				
GB4B-128, GB4C-128	1.0 uF X65 0402	2	4	Under GPU
	4.7 uF X65 0603	1	2	Near GPU
	10 uF X5R 0805	2	1	Midway between GPU and Power Supply
	22 uF X5R 0805	2	1	Midway between GPU and Power Supply
N16 PEX_IOVDD (N17 PEX_HVDD) Supply Rail				
GB4B-128, GB4C-128	1.0 uF X65 0402	2	4	Under GPU
	4.7 uF X65 0603	1	2	Near GPU
	10 uF X5R 0805	2	2	Midway between GPU and Power Supply
	22 uF X5R 0805	2	1	Midway between GPU and Power Supply

N17P VDD5
1uF*5/4.7uF*5 (under GPU)
330uF*1/22uF*3/10uF*2/4.7uF*2



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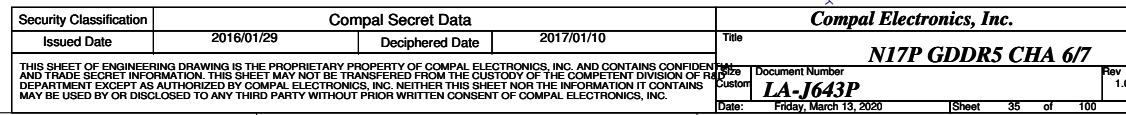
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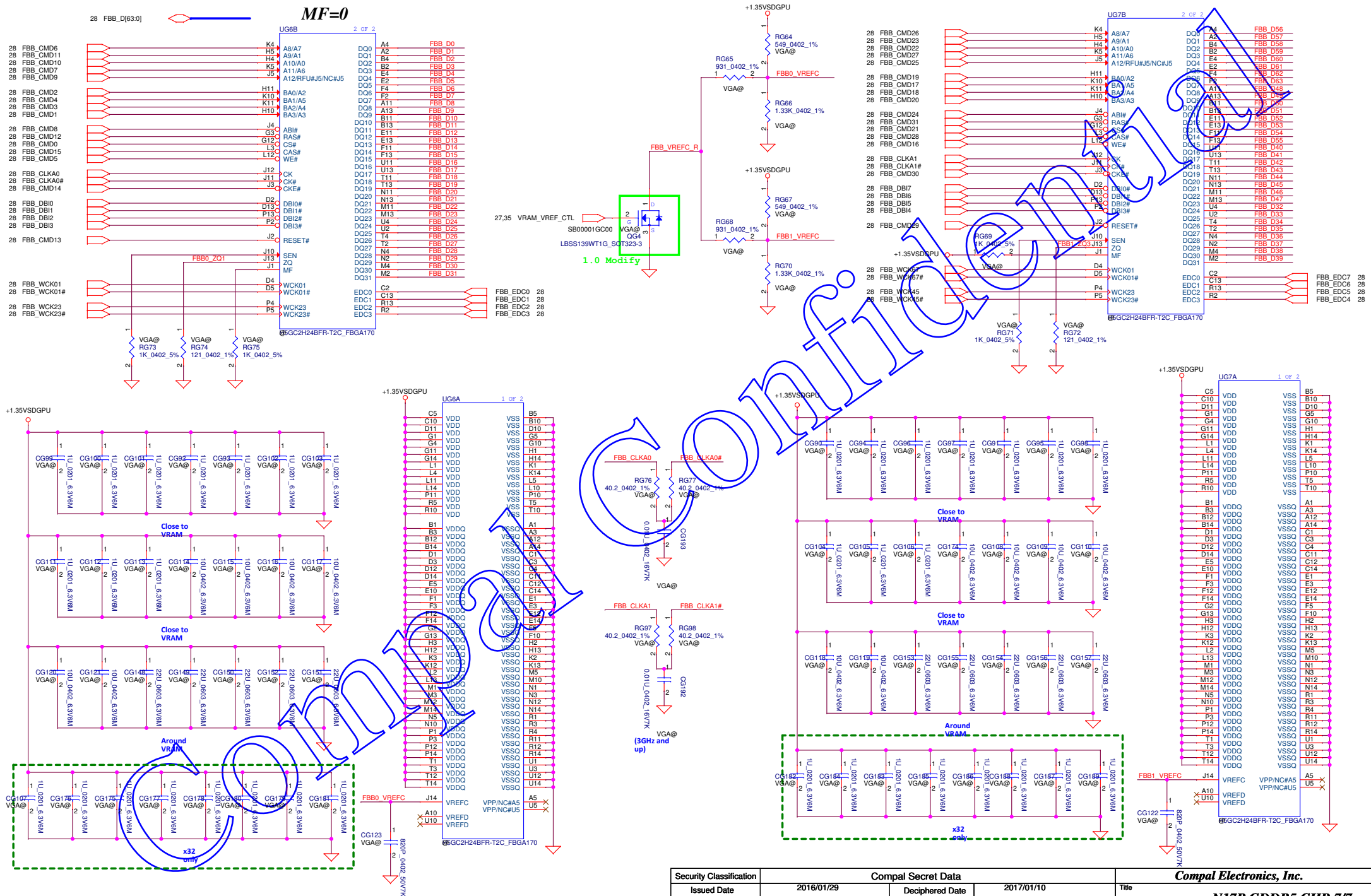
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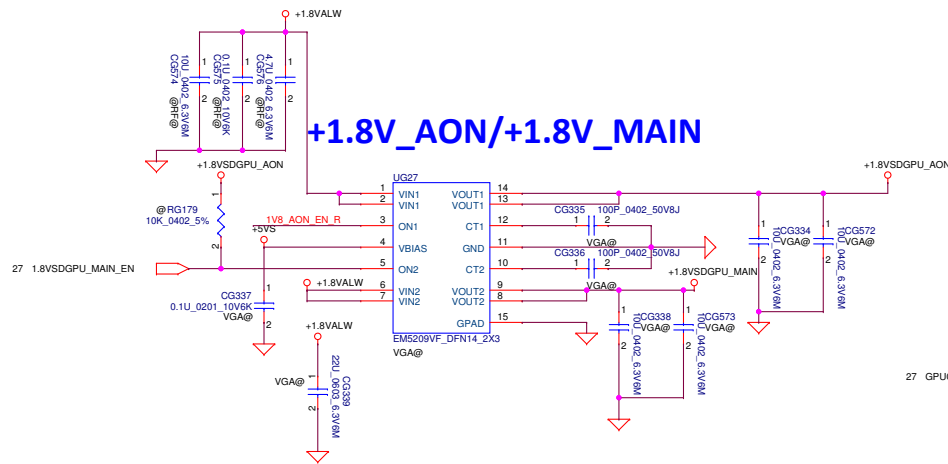
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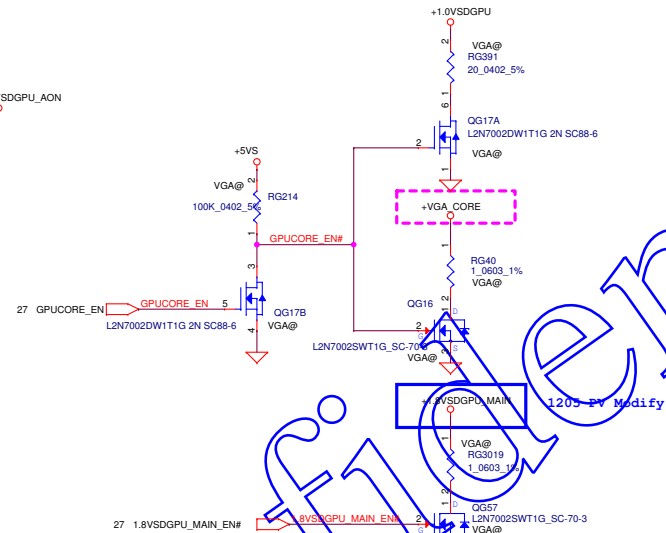
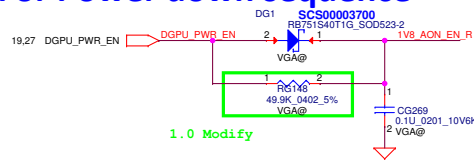
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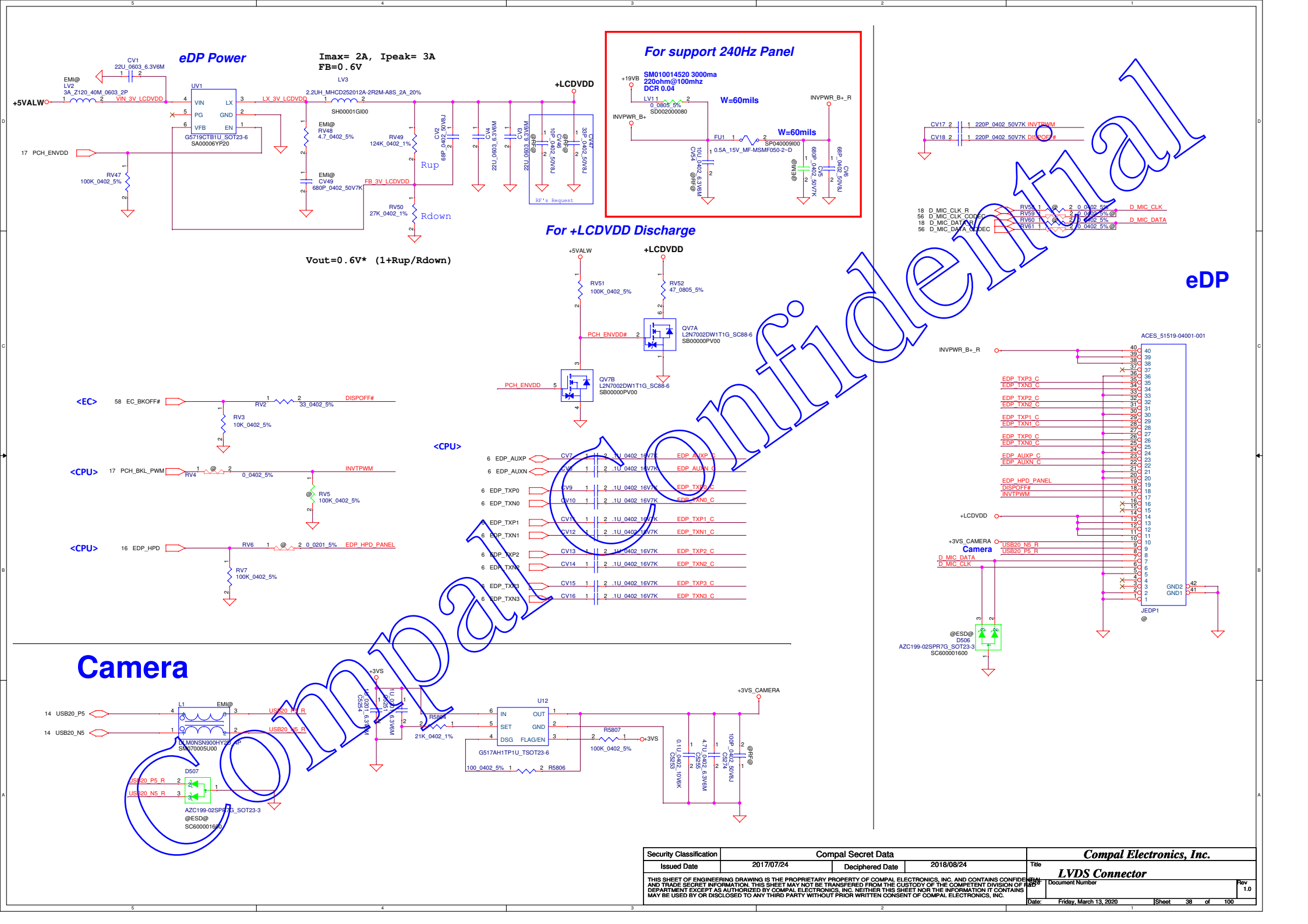




For Power down sequence



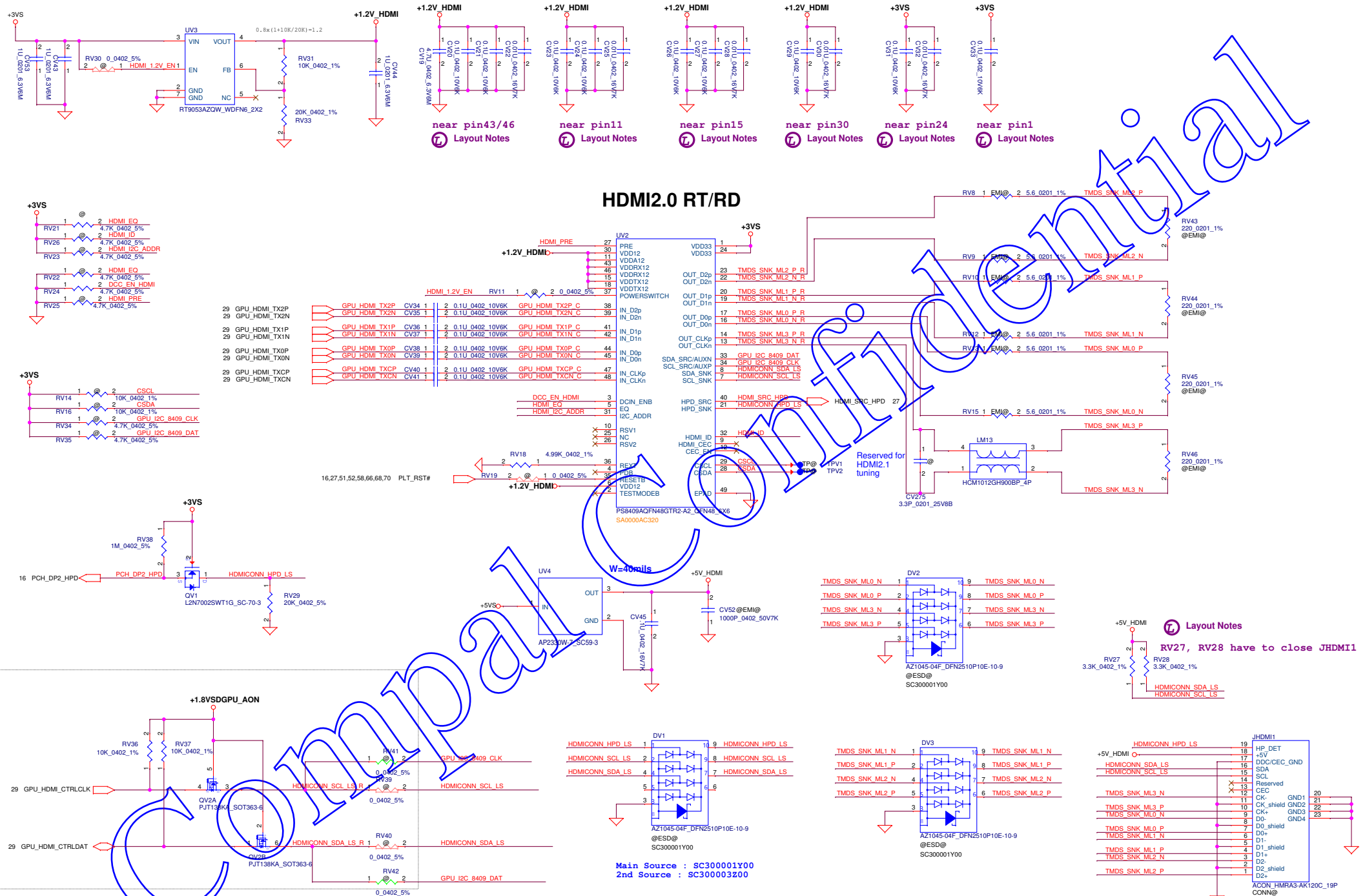
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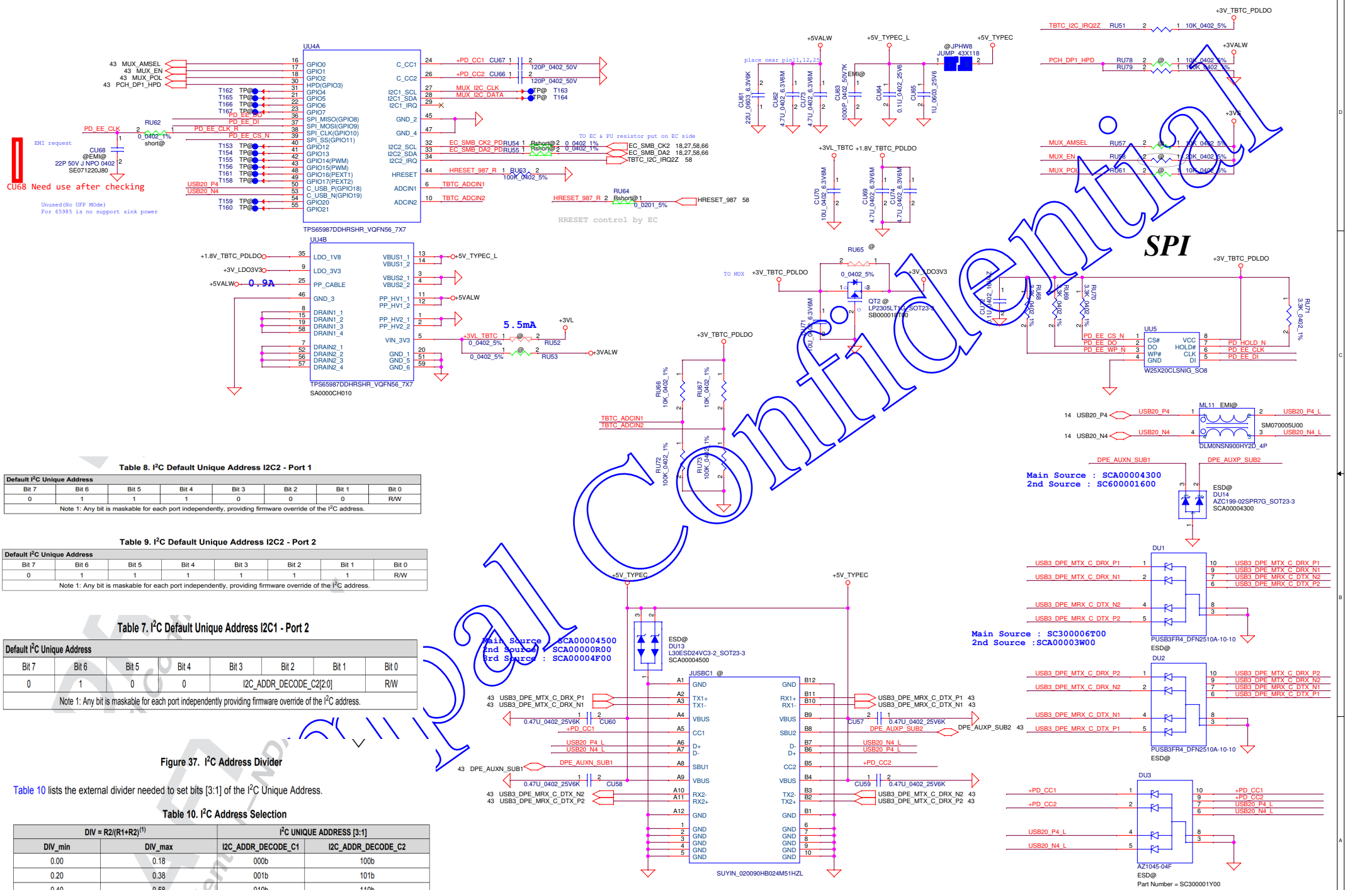


Table 8. I²C Default Unique Address I2C2 - Port 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	0	0	0	R/W

Note 1: Any bit is maskable for each port independently, providing firmware override of the I²C address.

Table 9. I²C Default Unique Address I2C2 - Port 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	1	1	1	R/W

Note 1: Any bit is maskable for each port independently, providing firmware override of the I²C address.

Table 7. I²C Default Unique Address I2C1 - Port 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0				R/W

Note 1: Any bit is maskable for each port independently providing firmware override of the I²C address.

Figure 37. I²C Address Divider

Table 10 lists the external divider needed to set bits [3:1] of the I²C Unique Address.

Table 10. I²C Address Selection

DIV = R2/(R1+R2) ⁽¹⁾		I ² C UNIQUE ADDRESS [3:1]	
DIV_min	DIV_max	I2C_ADDR_DECODE_C1	I2C_ADDR_DECODE_C2
0.00	0.18	000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
0.60	1.00	011b	111b

(1) External resistor tolerance of 1% is required. Resistor values should be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

GPIO/I2C mode

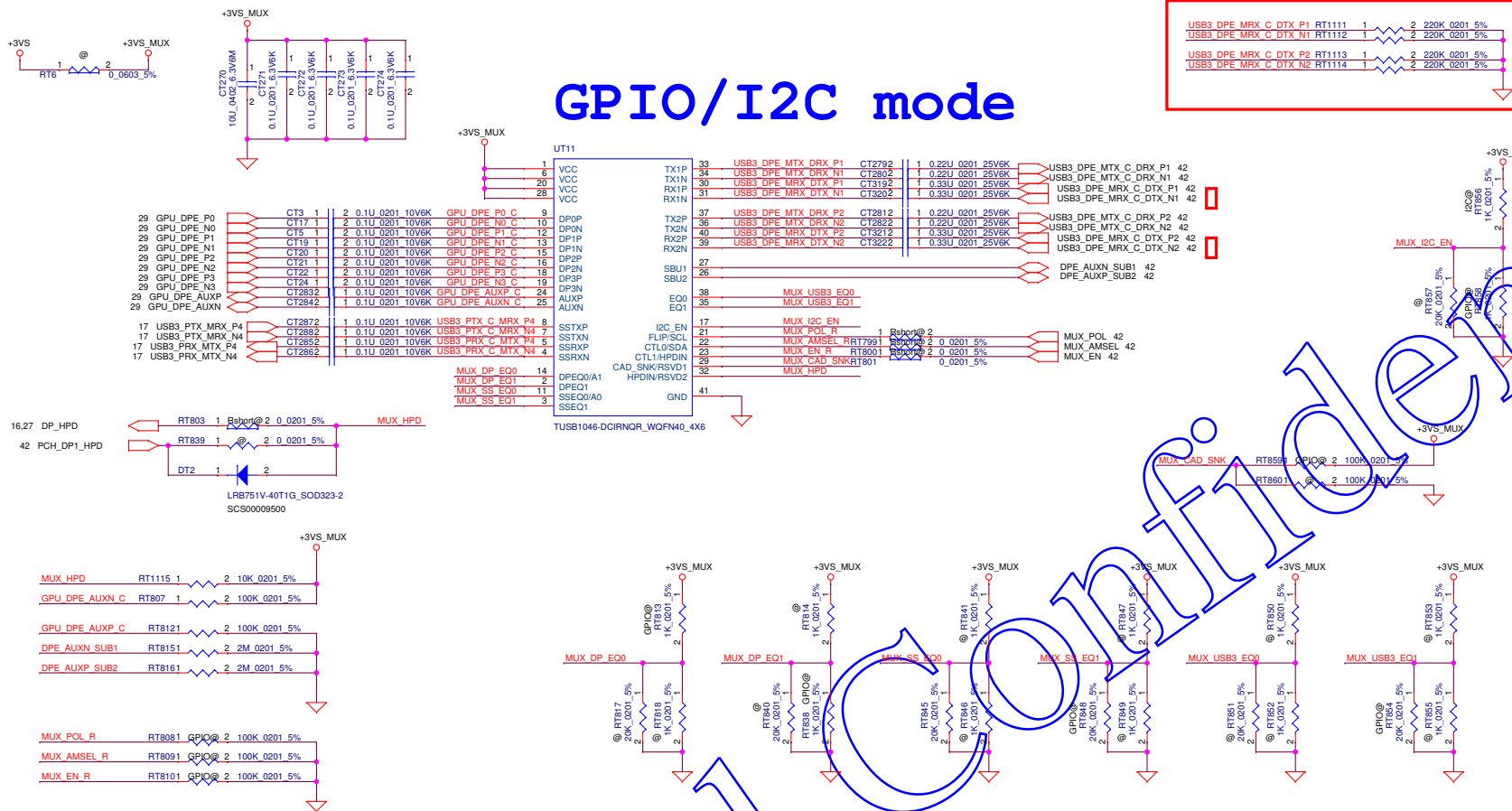


Table 7. USB1046-DCI Receiver Equalization GPIO Control

Equalization Setting #	USB3.1 DOWNSTREAM FACING PORTS			USB 3.1 UPSTREAM FACING PORT			ALL DISPLAYPORT LANES		
	EQ1 PIN LEVEL	EQ0 PIN LEVEL	EQ GAIN at 5 GHz (dB)	SSEQ1 PIN LEVEL	SSEQ0 PIN LEVEL	EQ GAIN at 5 GHz (dB)	DPEQ1 PIN LEVEL	DPEQ0 PIN LEVEL	EQ GAIN at 4.05 GHz (dB)
0	0	0	-3.9	0	0	-1.8	0	0	1.0
1	0	R	-1.7	0	R	0.2	0	R	3.3
2	0	F	-0.1	0	F	1.7	0	F	4.9
3	0	1	1.4	0	1	3.2	0	1	6.5
4	R	0	2.4	R	0	4.2	R	0	7.5
5	R	R	3.5	R	R	5.3	R	R	8.6
6	R	F	4.4	R	F	6.1	R	F	9.5
7	R	1	5.2	R	1	7.0	R	1	10.4
8	F	0	5.9	F	0	7.7	F	0	11.1
9	F	R	6.6	F	R	8.3	F	R	11.7
10	F	F	7.1	F	F	8.8	F	F	12.3
11	F	1	7.6	F	1	9.3	F	1	12.8
12	1	0	8.0	1	0	9.7	1	0	13.2
13	1	R	8.5	1	R	10.1	1	R	13.6
14	1	F	8.8	1	F	10.4	1	F	14.0
15	1	1	9.2	1	1	10.8	1	1	14.4

Table 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 KΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 KΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 KΩ 5% to V _{CC} . Option 2: Tie directly to V _{CC} .

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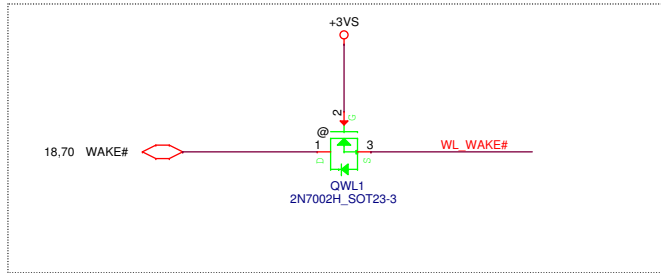
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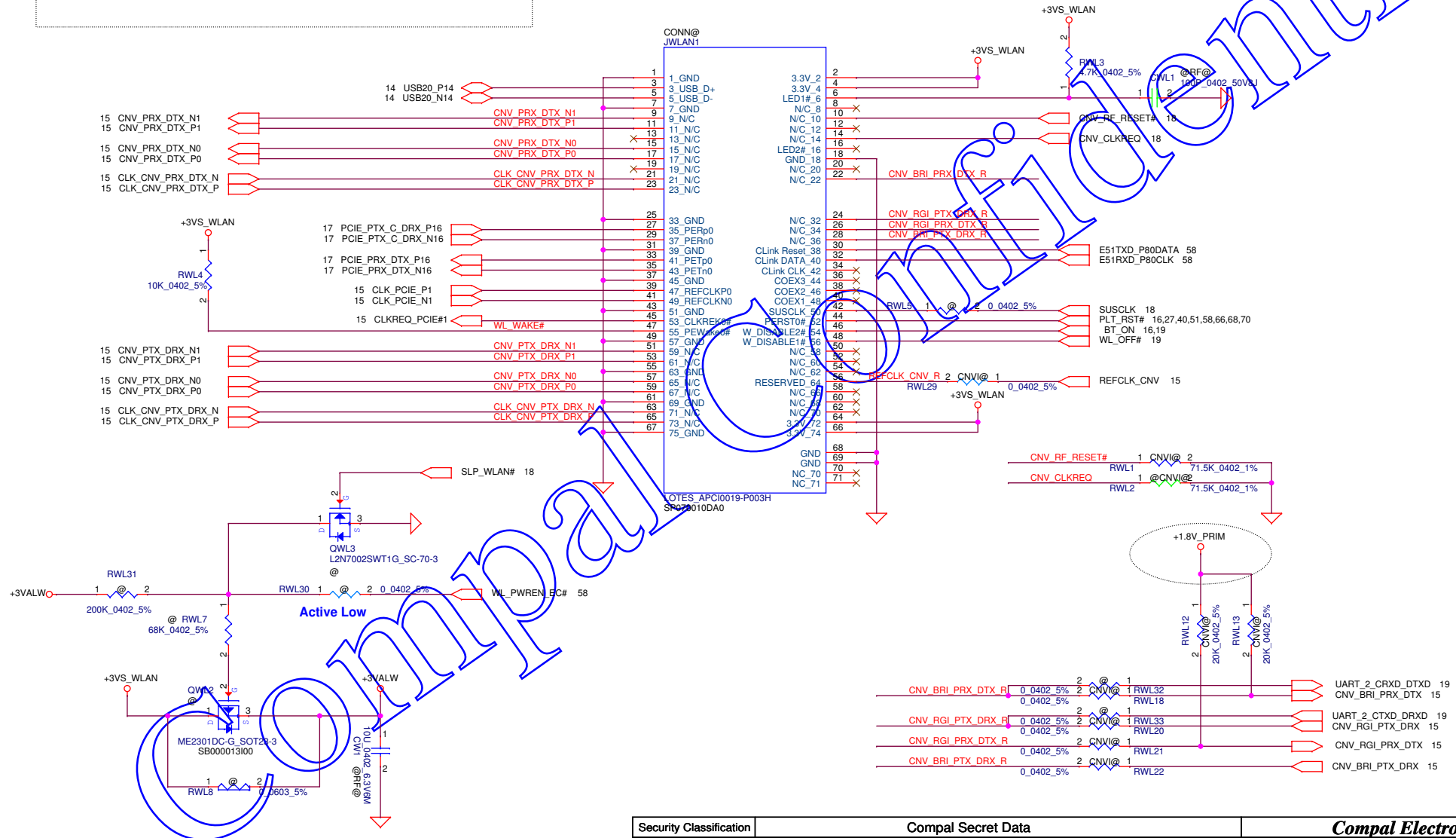
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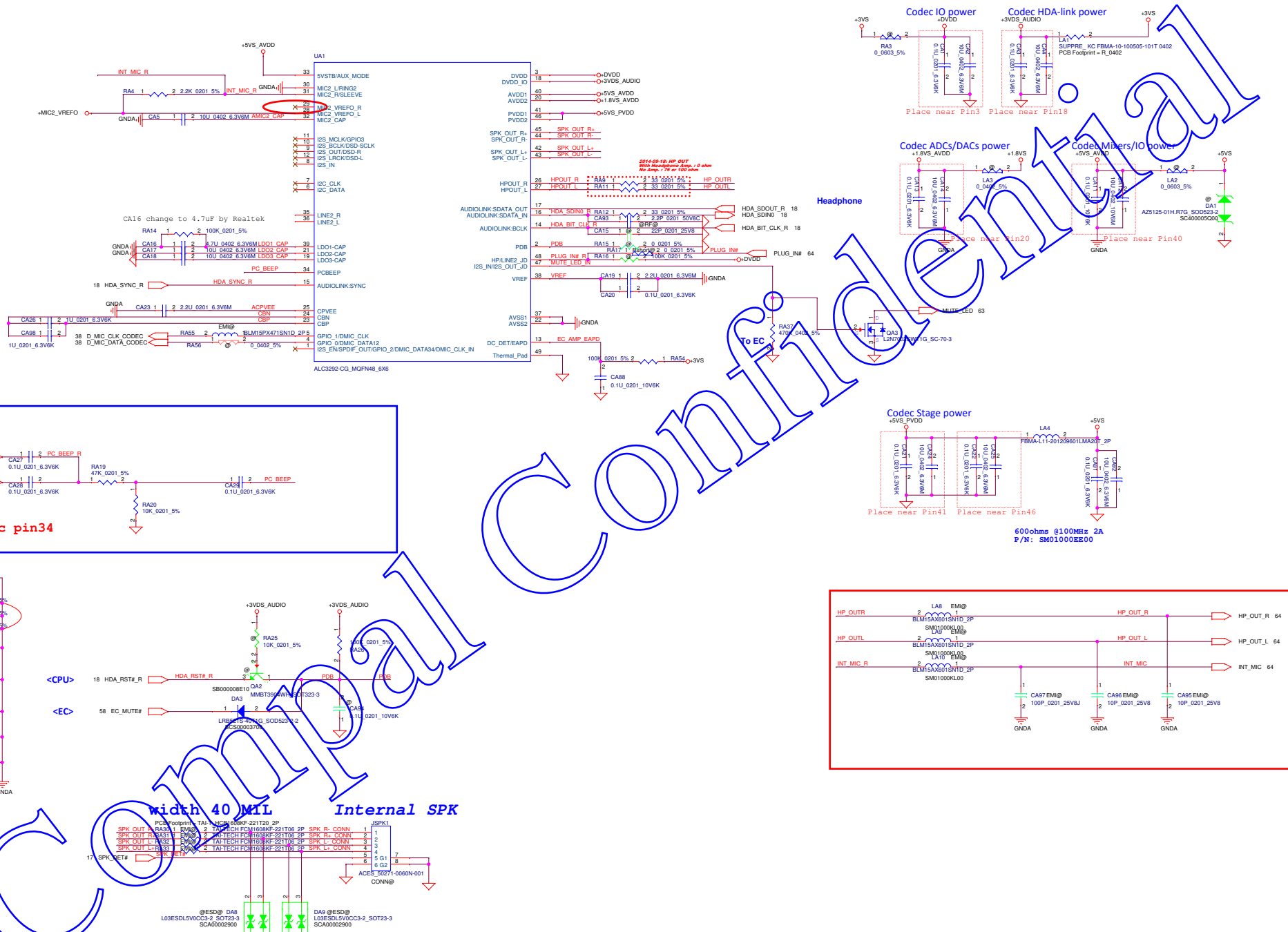
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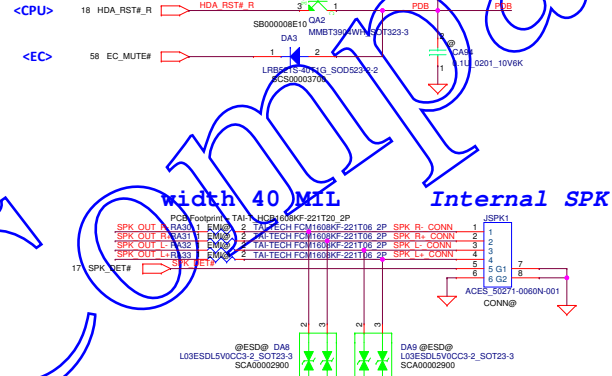
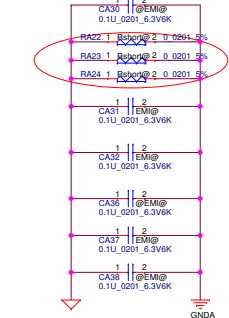


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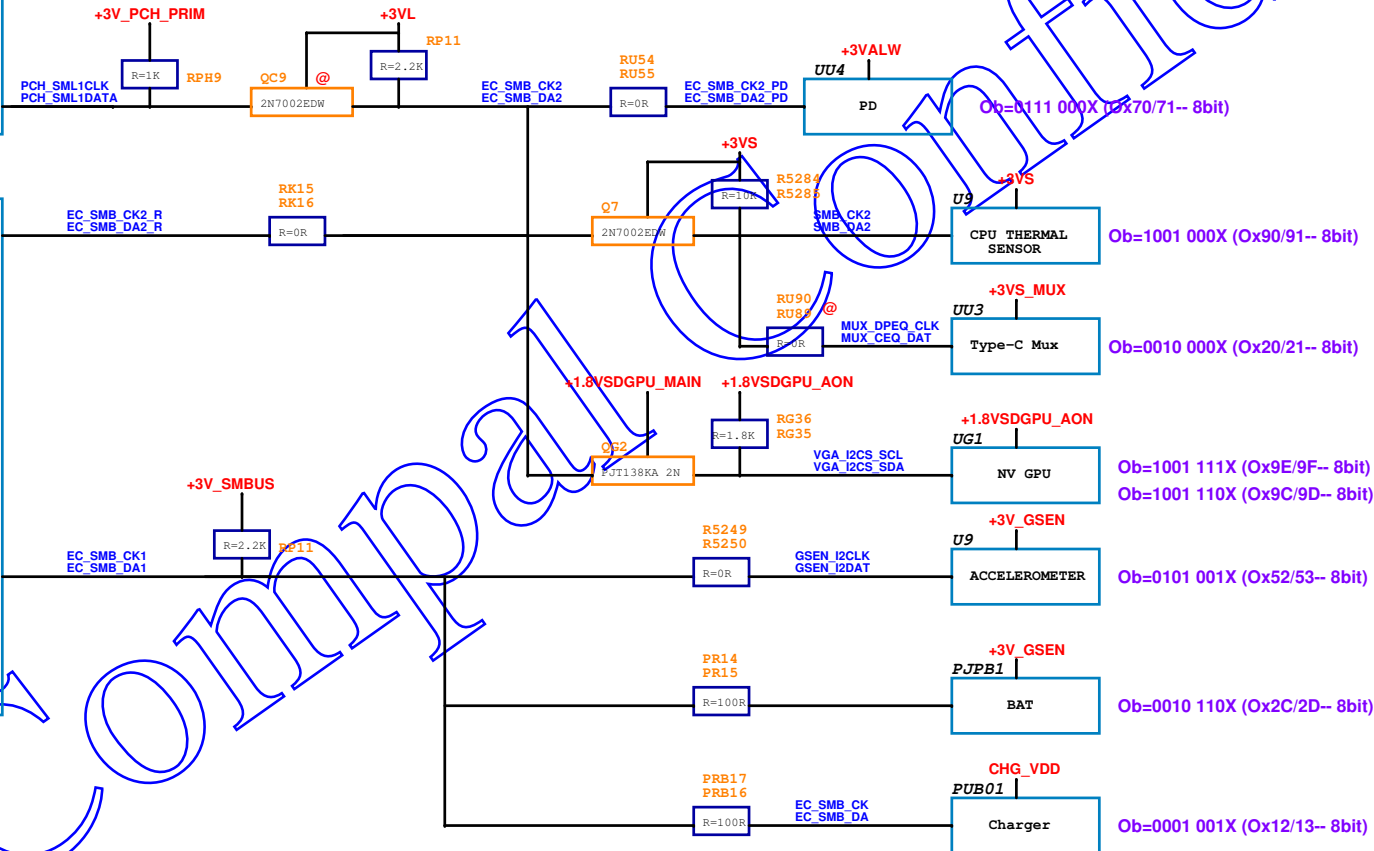
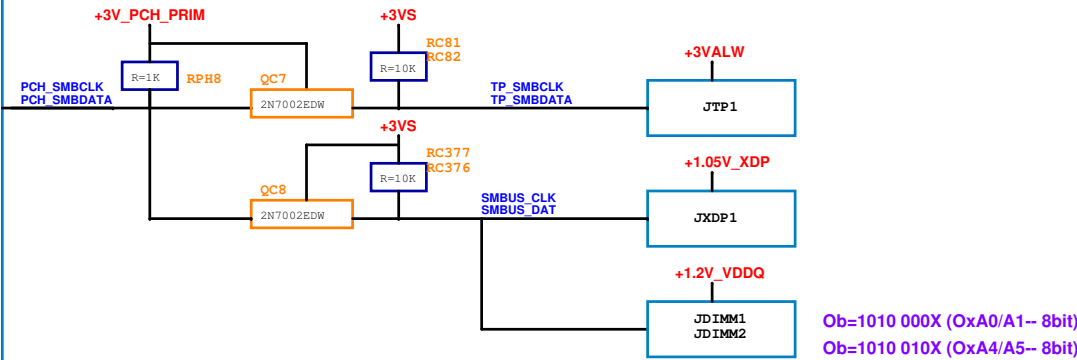
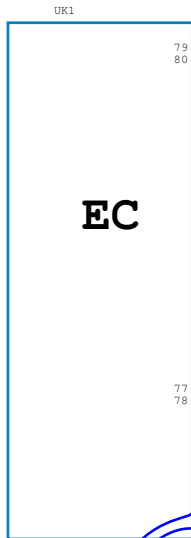
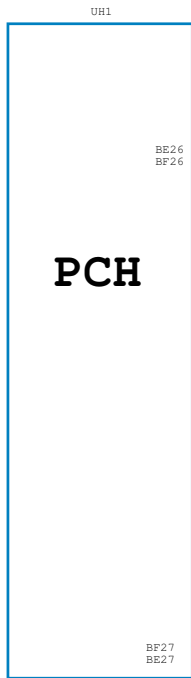
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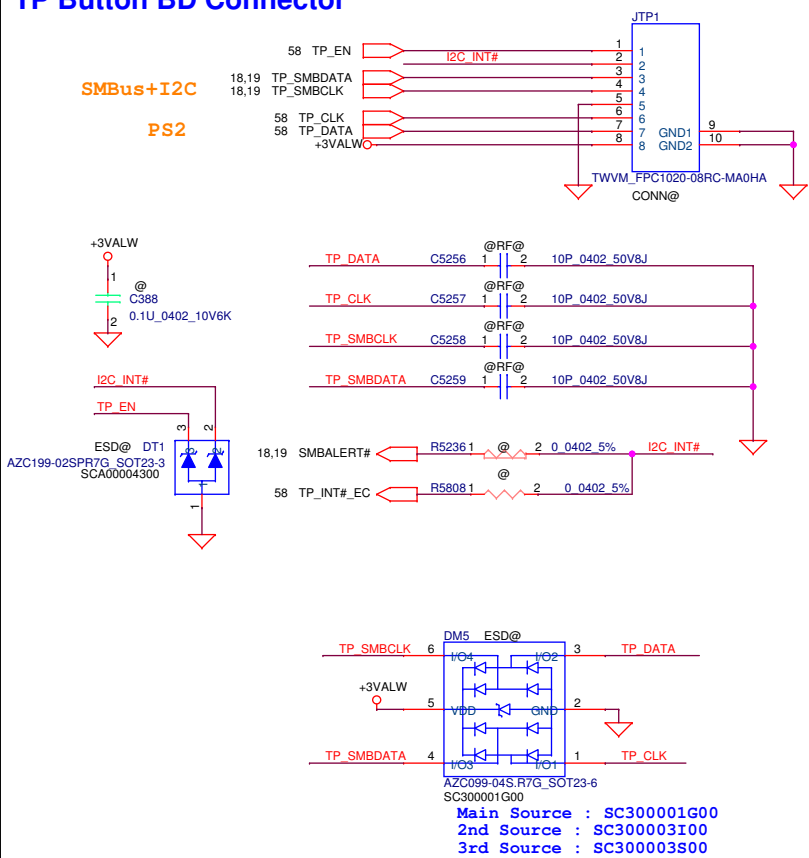


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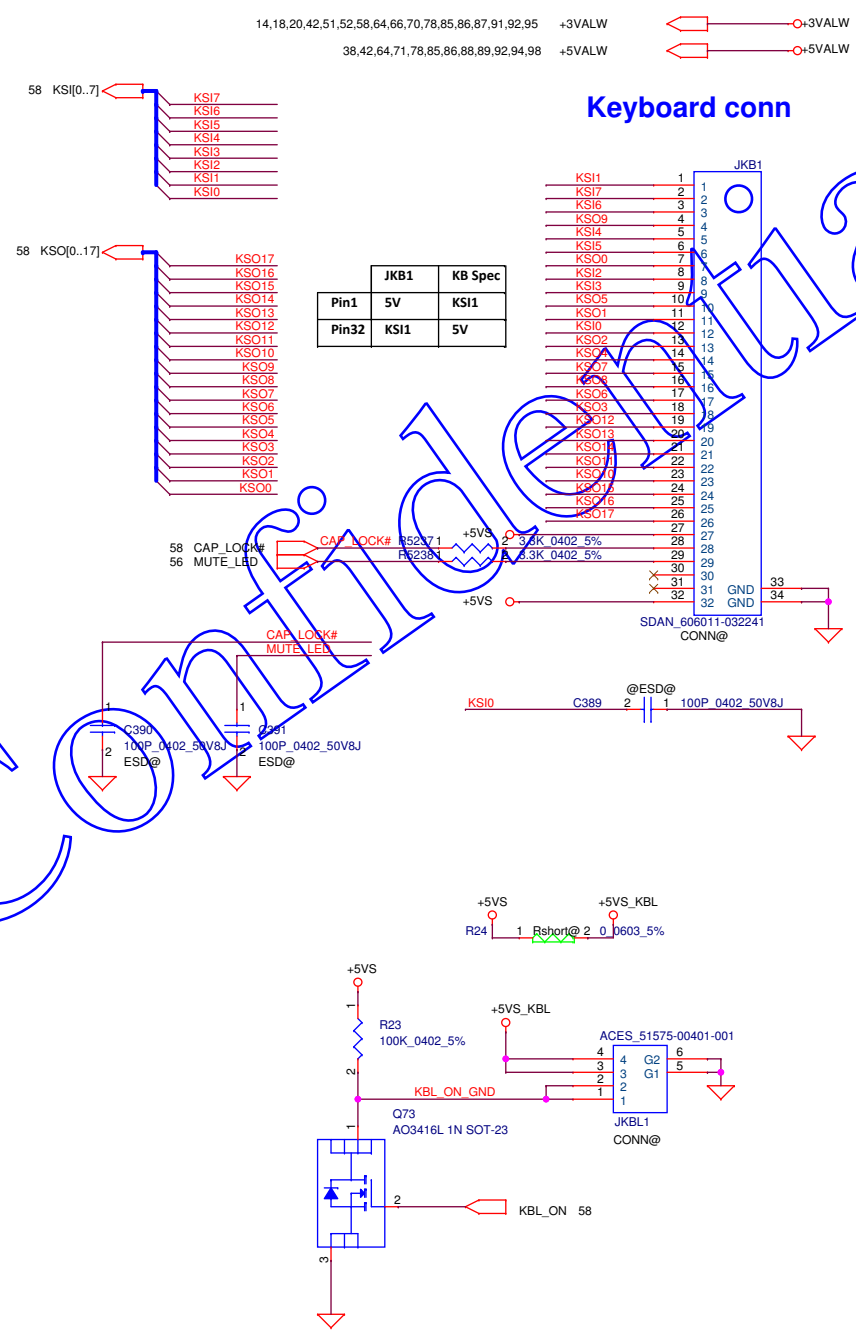
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TP Button BD Connector

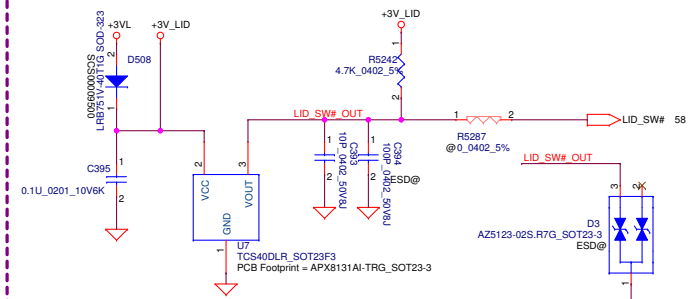


Pin Assignment and Description			
Pin#	Signal	I/O	Description
1	VDD_3.3V	Power	3.3V +/-5%. Power ripple: 100 mVpp max. Power sequence: See section 4.6.
2	PS2_DATA	I/O	PS2 data
3	PS2_CLK	I/O	PS2 clock
4	GND	GND	Ground
5	SMB_CLK	I/O	SMBUS clock $I_{ON} \text{ or } I_{OFF}$: 8 mA max.
6	SMB_DATA	I/O	SMBUS data. $I_{ON} \text{ or } I_{OFF}$: 8 mA max.
7	/INT (/ATTN)	0	For SMBus application, low active, Indicates touchpad likes to send data to system (host) if go low.
8	LID_CLOSE (TP Disable/Enable)	I	Enable or disable touchpad, low active Low: Disable TP High: Enable TP

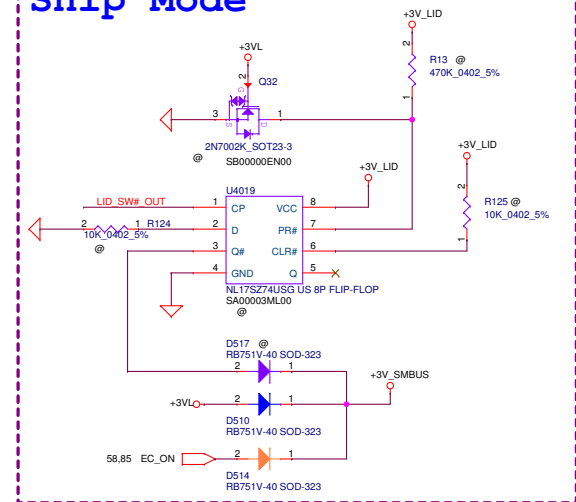


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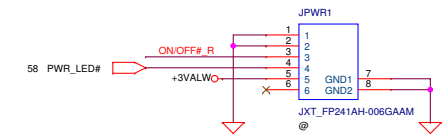
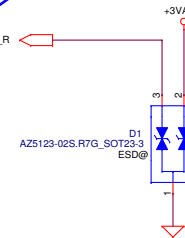
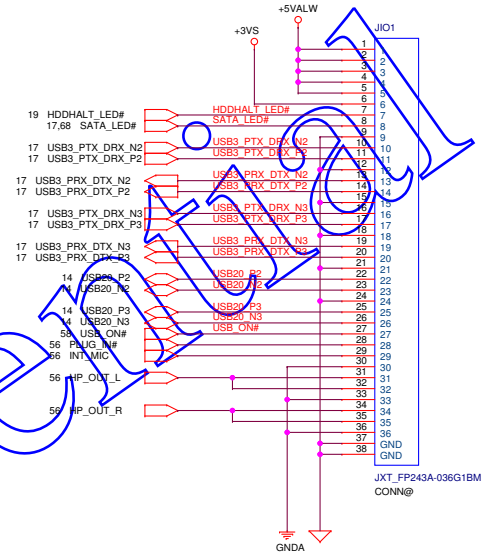
Lid Switch (Hall Effect Sensor)



Ship Mode



To IO Board



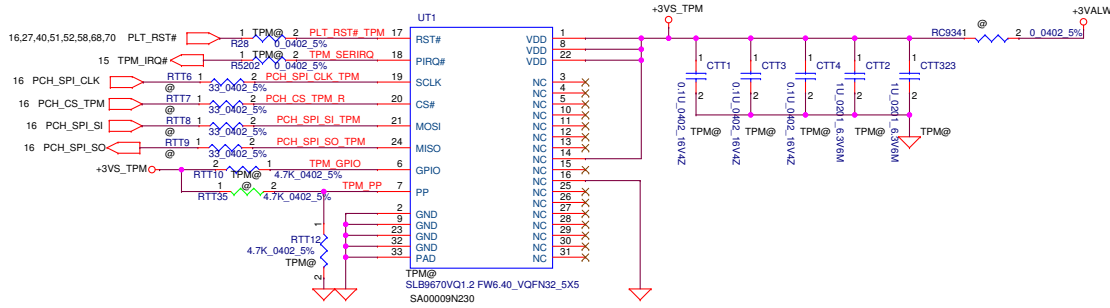
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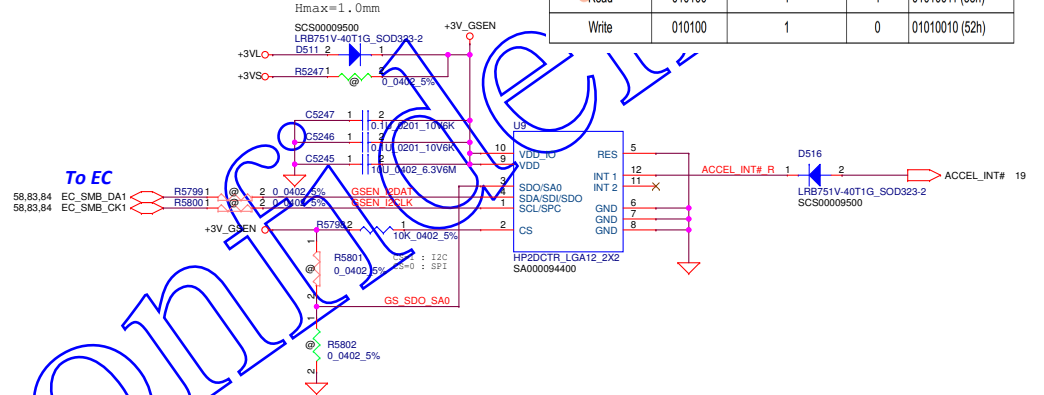
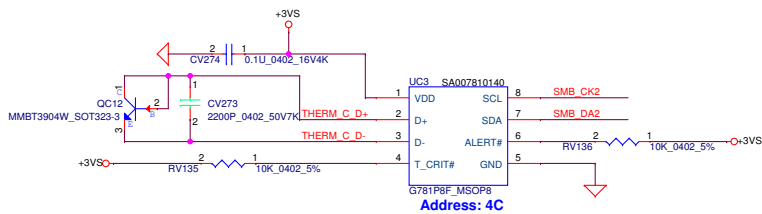


ACCELEROMETER ST Micro HP2DC

Table 12. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

CPU THERMAL SENSOR



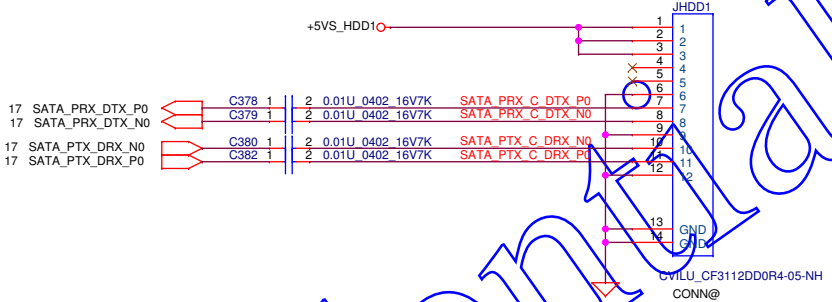
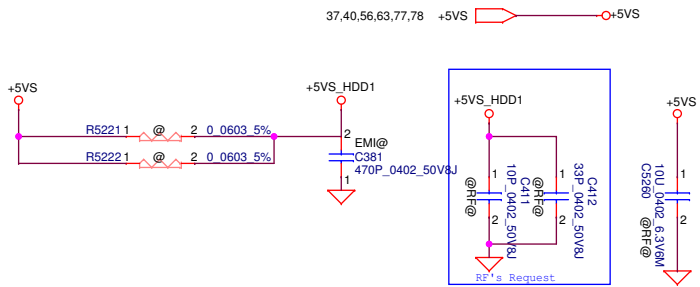
Slave Address

The G753 appears to the SMBus as one device having a common address for both ADC channels.
The G753 has the following SMBus slave address:

	A6	A5	A4	A3	A2	A1	A0
G753	1	0	0	1	0	0	0

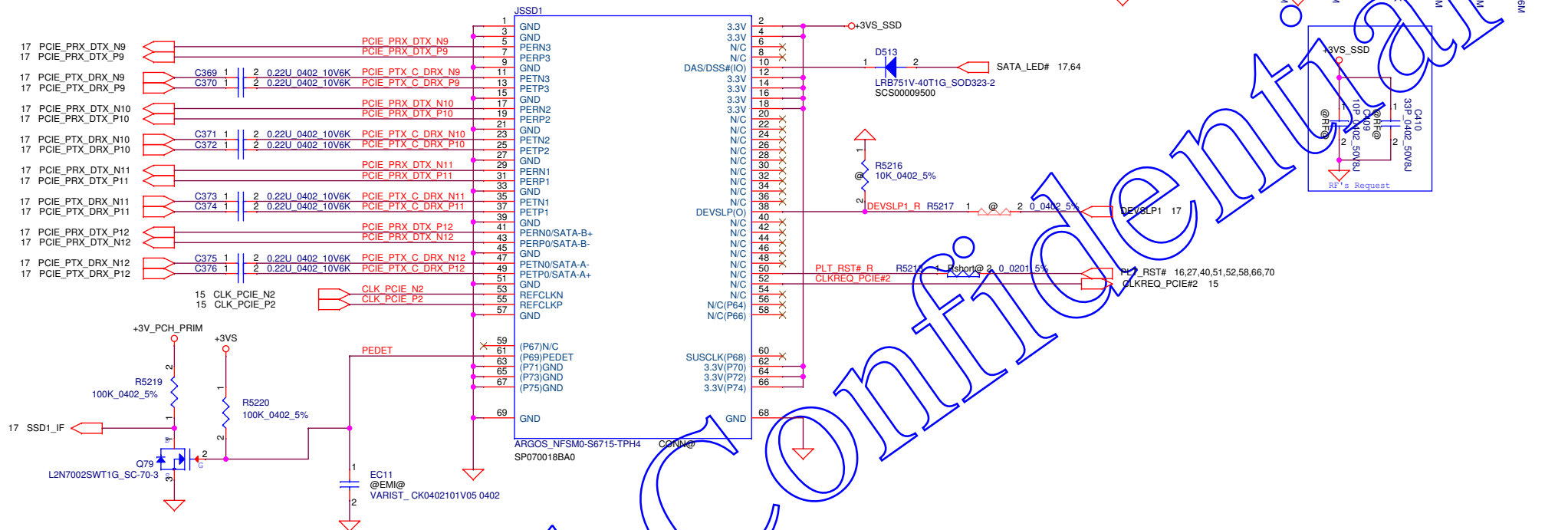
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2.5" SATA HDD



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										Rev	
										1.0	
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										Sheet 67 of 100	

M.2 SSD

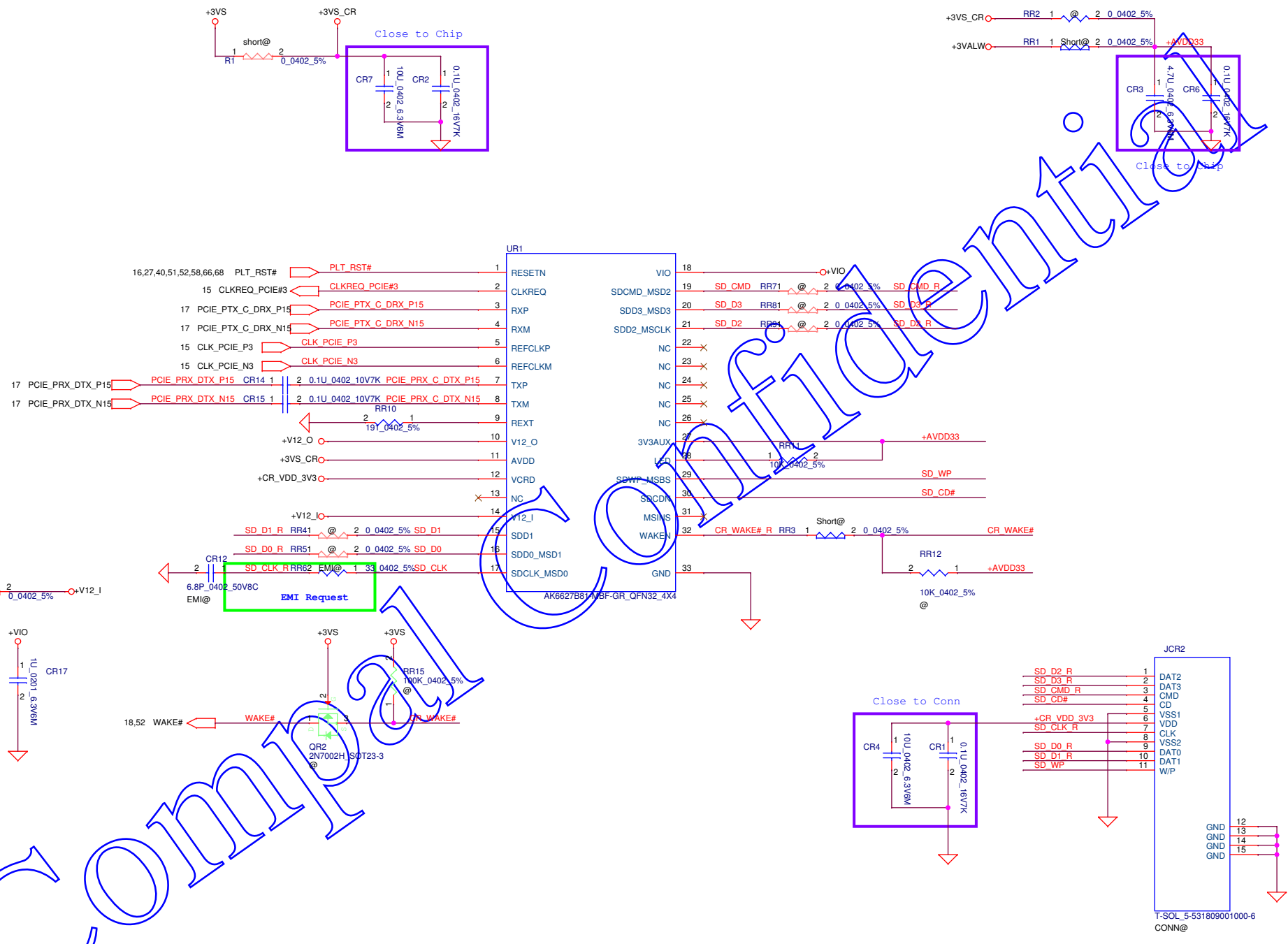


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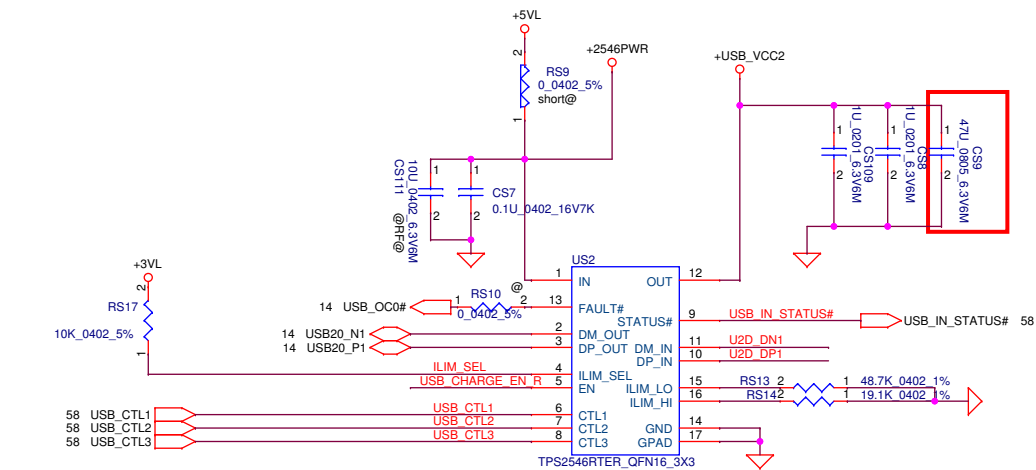
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2014-10-13: Change Correct Power Net Name
B+ => +19VB

2014-10-21: Change from single load switch back to MOS.
Load Switch have body diode will leakage from out to in.

2014-10-20: Change USB_IN_STATUS# PU to +3VL
(same power level as EC)

+19VB

2014-10-20: Change USB_IN_STATUS# PU to +3VL
(same power level as EC)
Pixar PV# 2013.01.07 Change
+VL to B+ to prevent
leakage

<EC> 58 USB_CHARGE_EN short@ RS16 1 2 0.0402 5% USB_CHARGE_EN_R

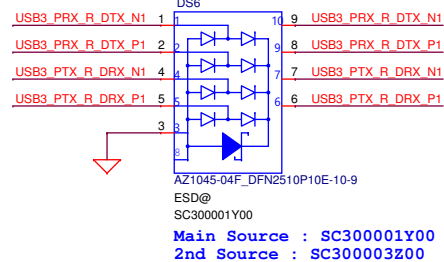
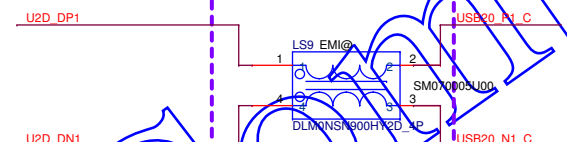
SPOK# 2 RS40 1 100K 0402 5%
USB_CTL1 2 RS41 1 100K 0402 5%
USB_CTL2 2 RS42 1 100K 0402 5%
USB_IN_STATUS# 2 RS43 1 100K 0402 5%

17 USB3_PTX_DRX_P1 USB3_PTX_DRX_P1 2 1 CS29 USB3_PTX_C_DRX_P1 RS28 1 2 0.0201 5% USB3_PTX_R_DRX_P1

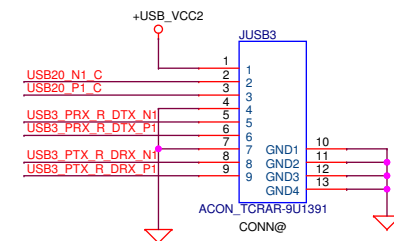
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17 USB3_PTX_DRX_P1 RS32 1 2 0.0201 5% USB3_PTX_R_DRX_P1

17 USB3_PTX_DRX_N1 RS34 1 2 0.0201 5% USB3_PTX_R_DRX_N1



USB2.0/USB3.0 port 2



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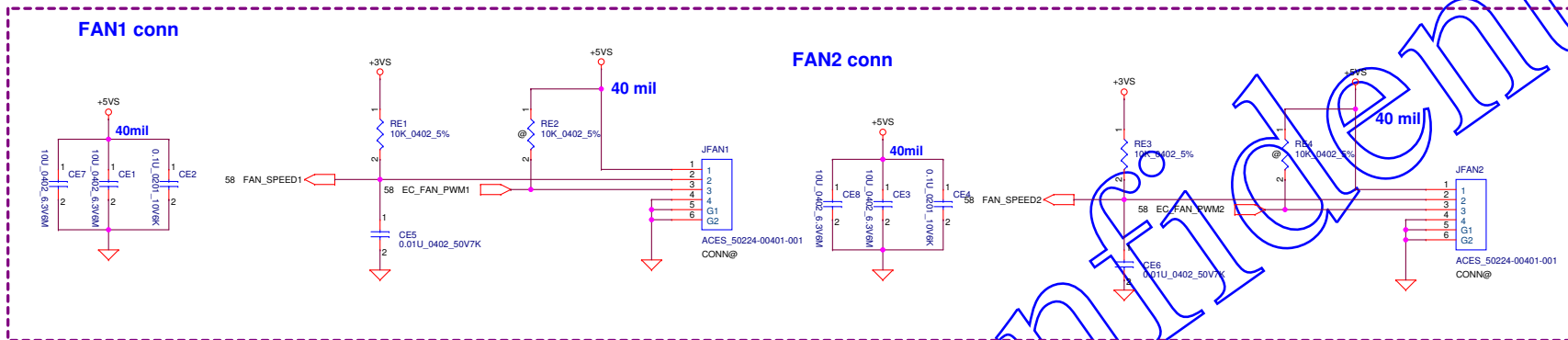
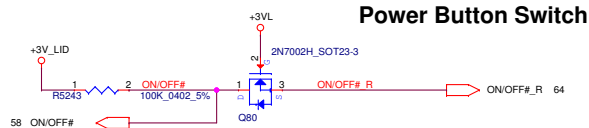
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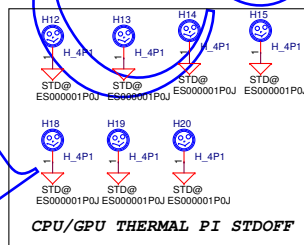
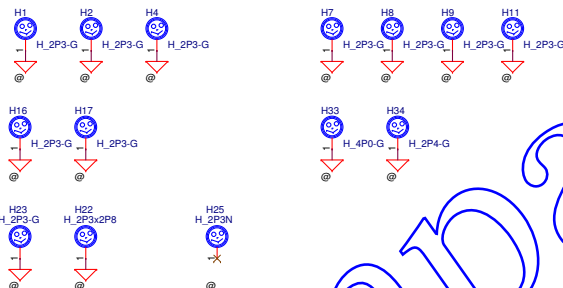
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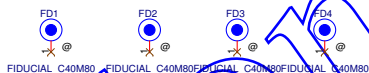
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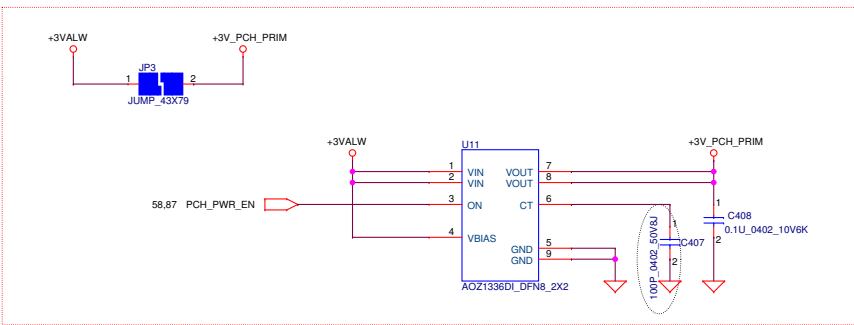
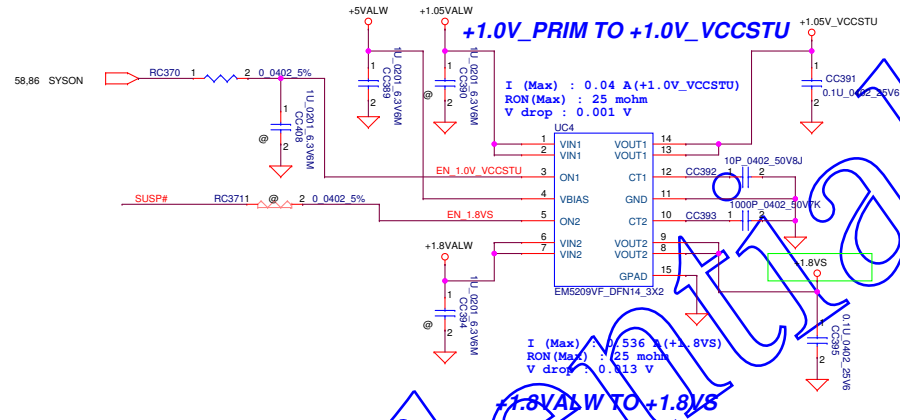
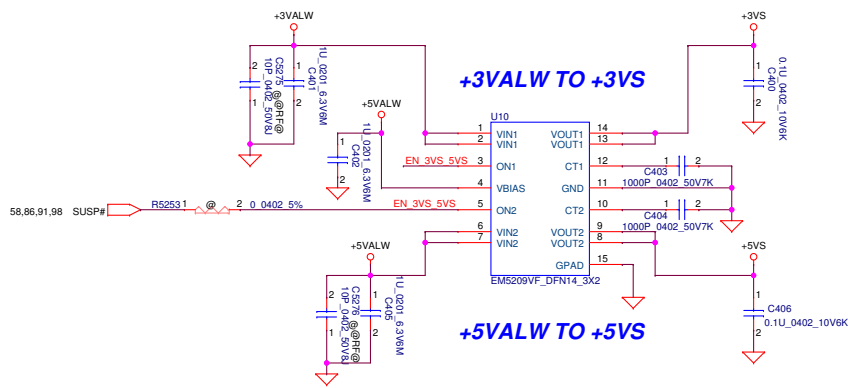
PCB Screw Hole



Fiducial Mark

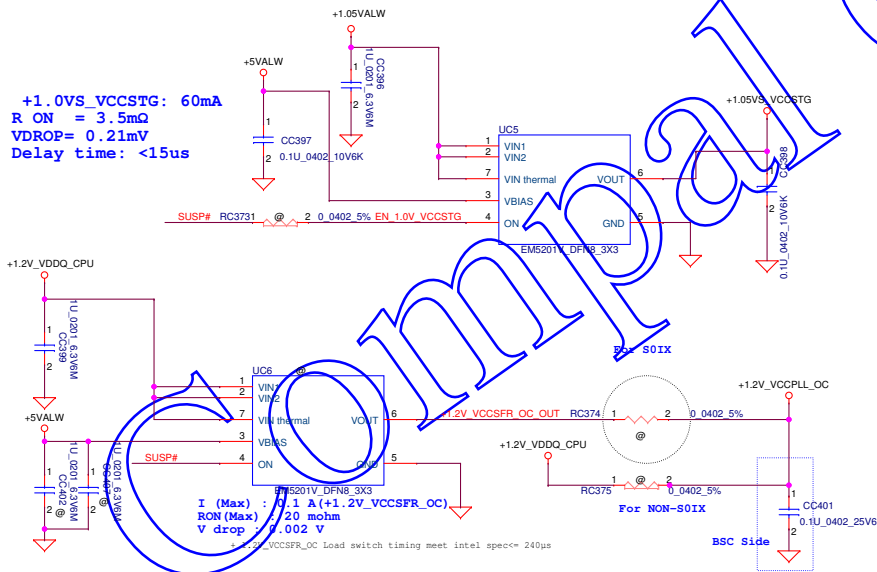


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+1VALW TO +1.0VS_VCCSTG

+1.0VS_VCCSTG: 60mA
R ON = 3.5mΩ
V DROP = 0.21mV
Delay time: <15us



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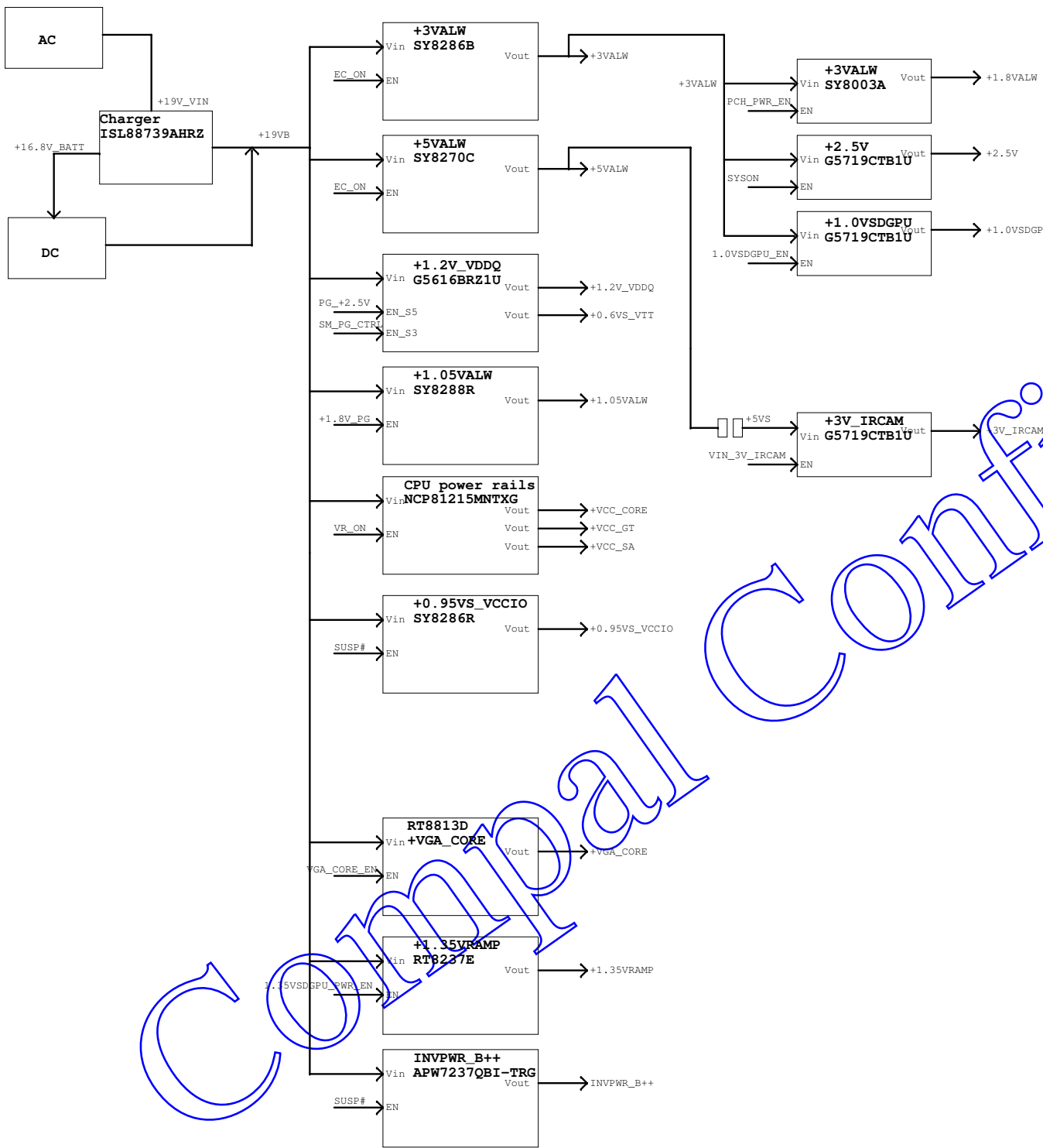
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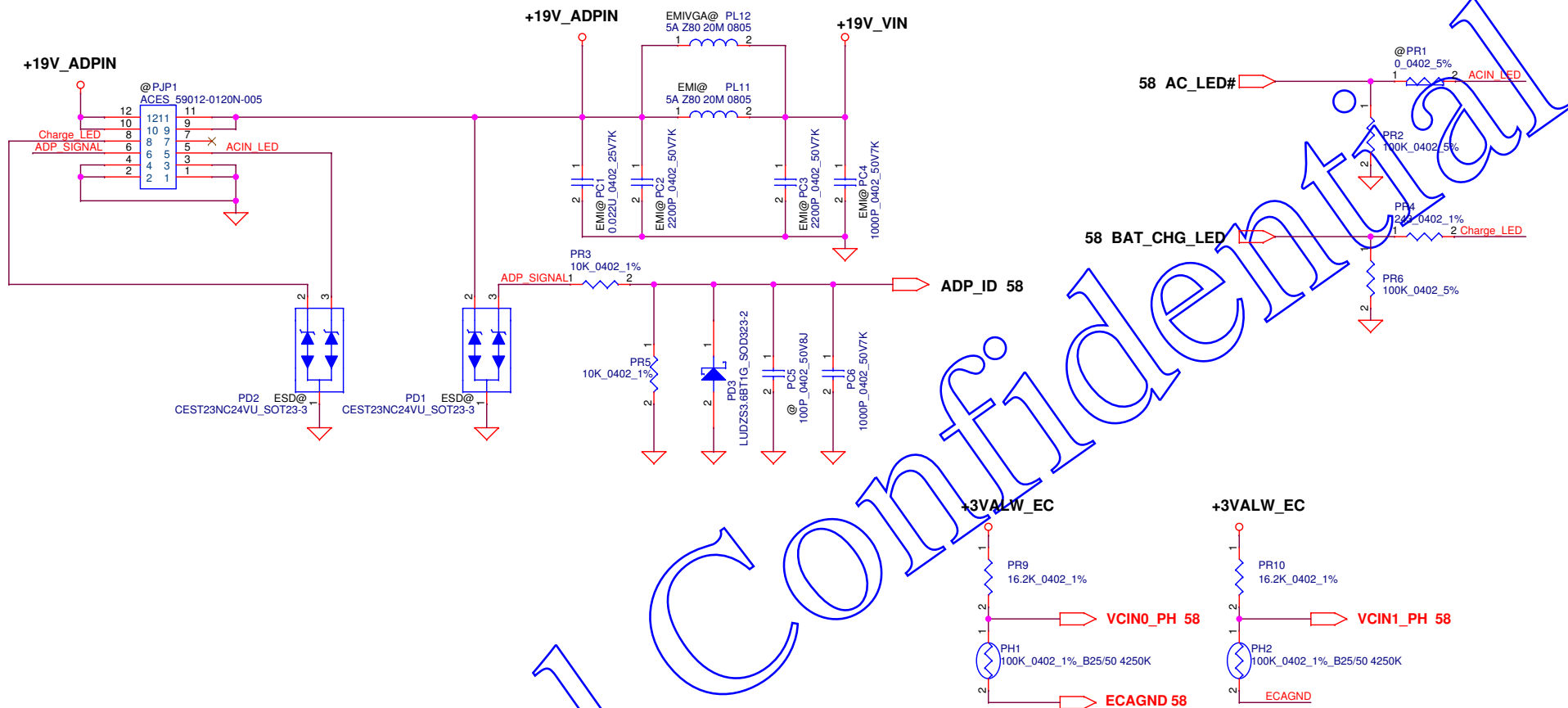
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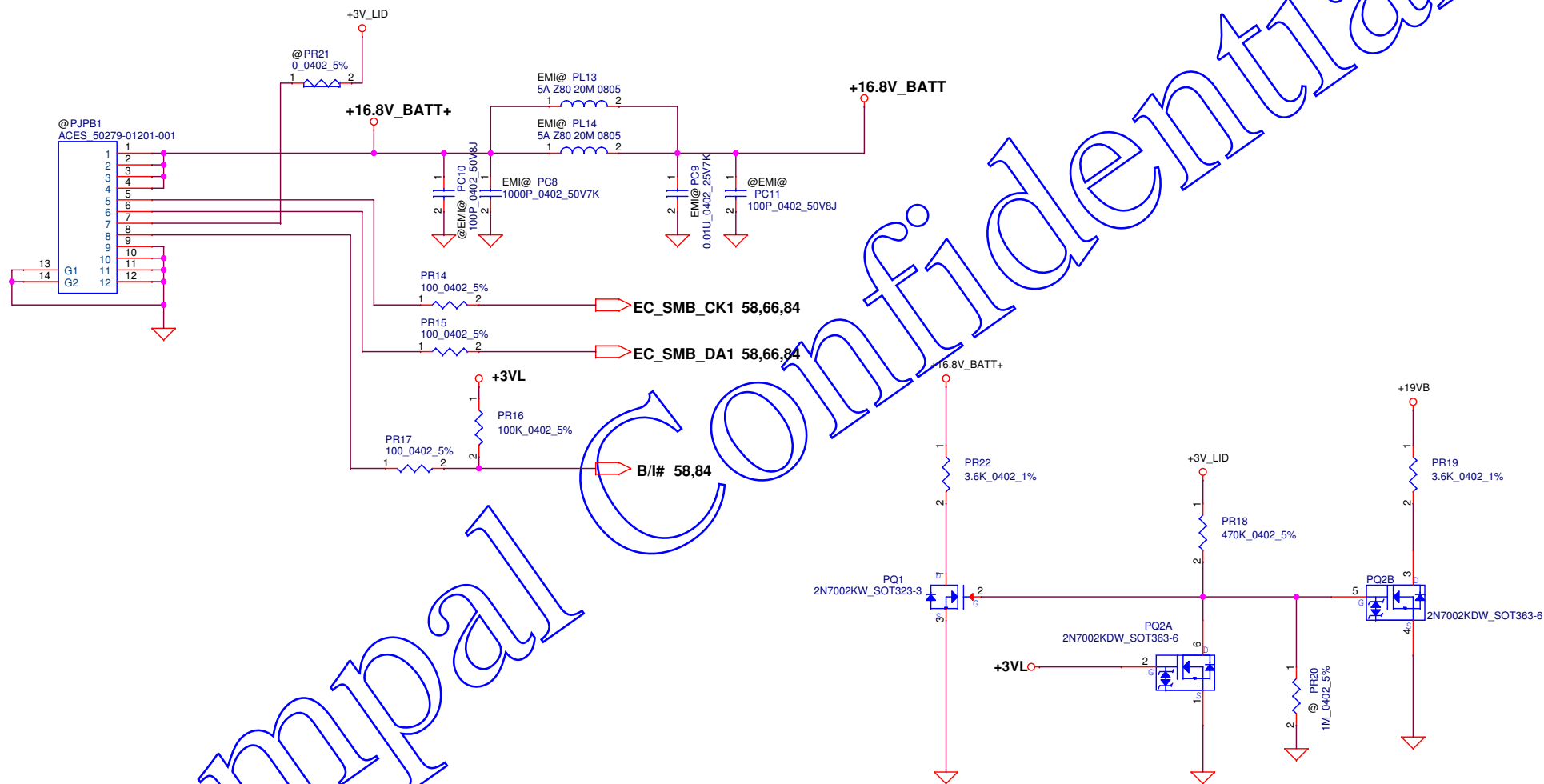
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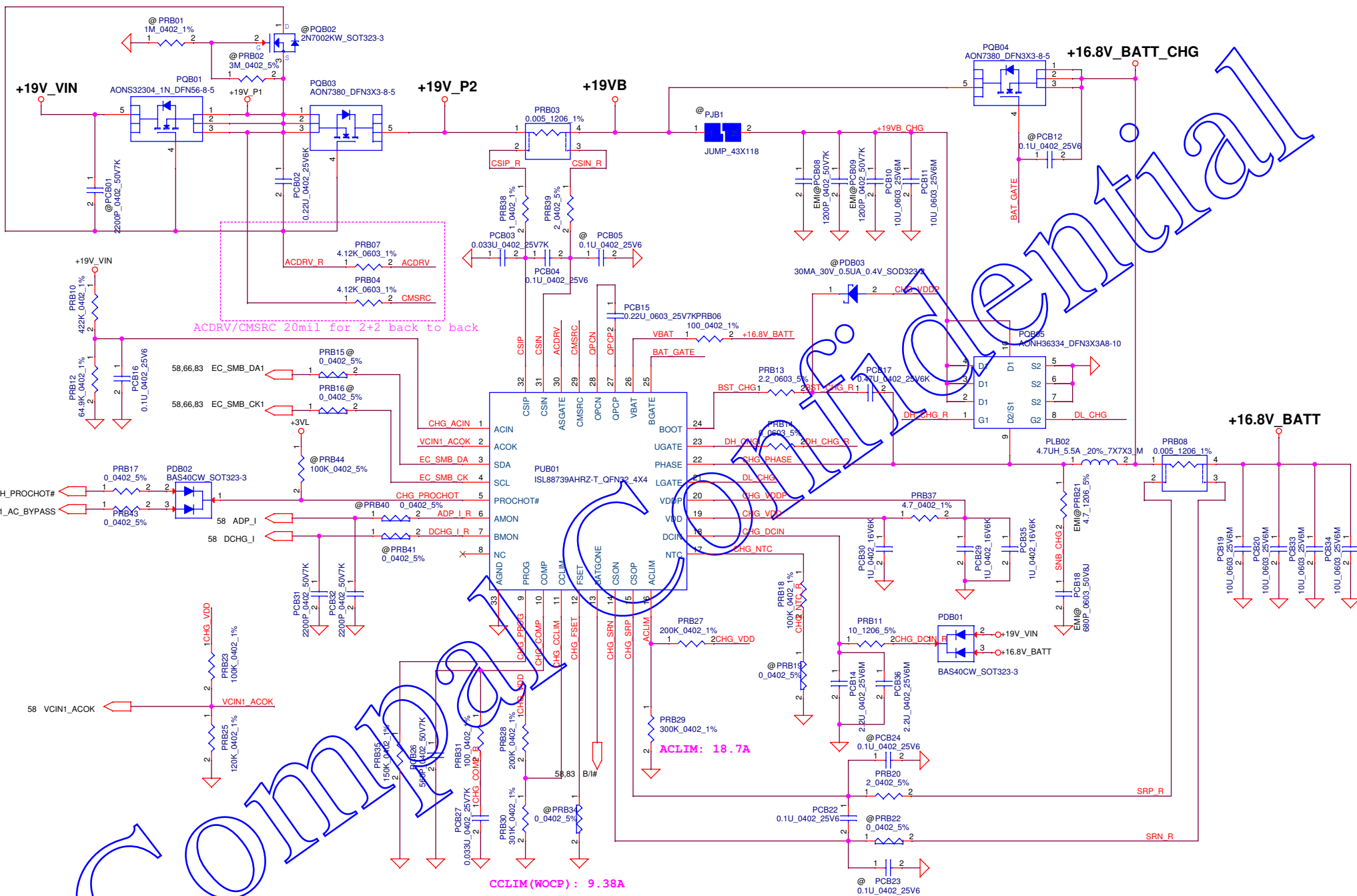




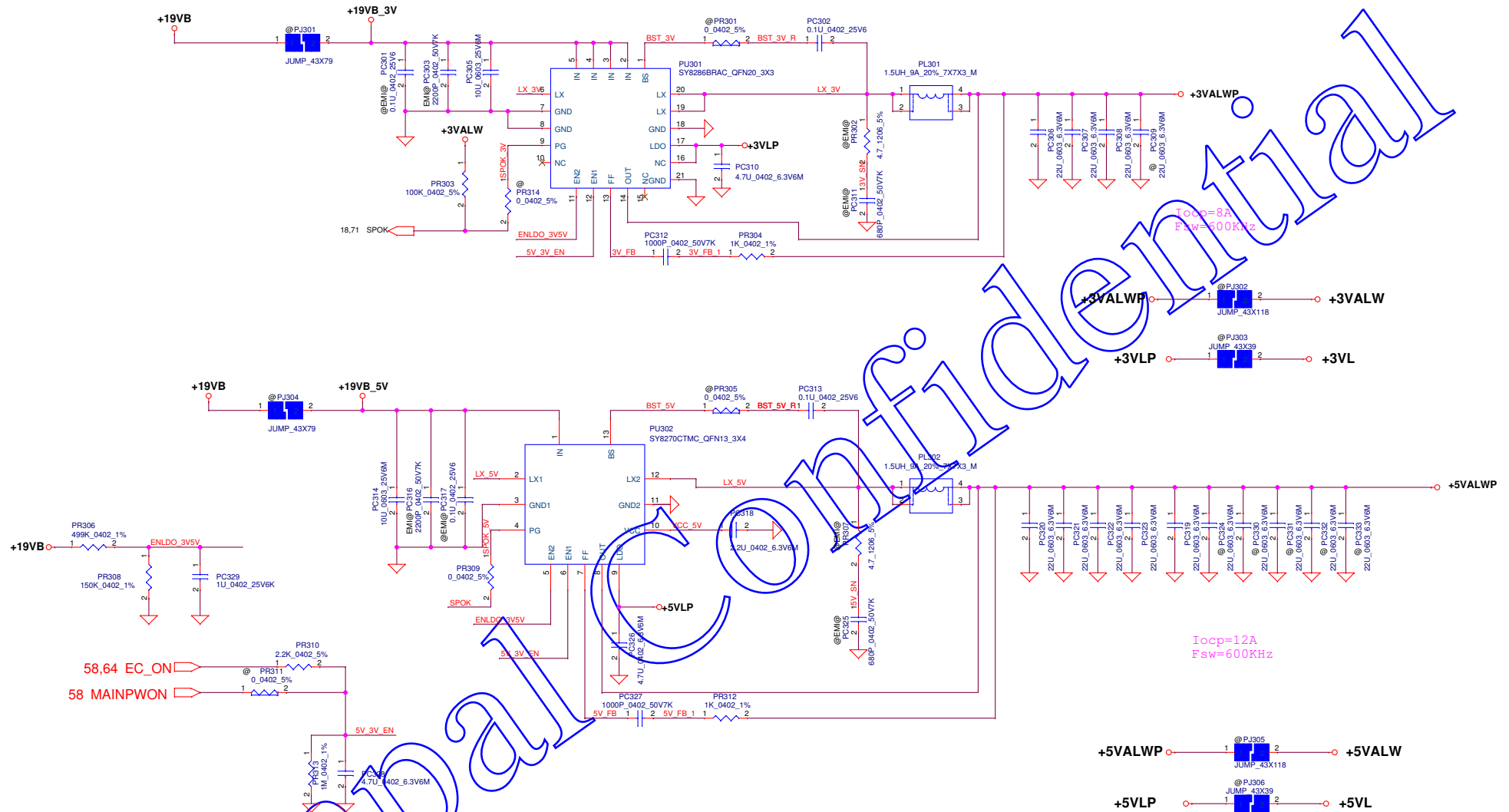
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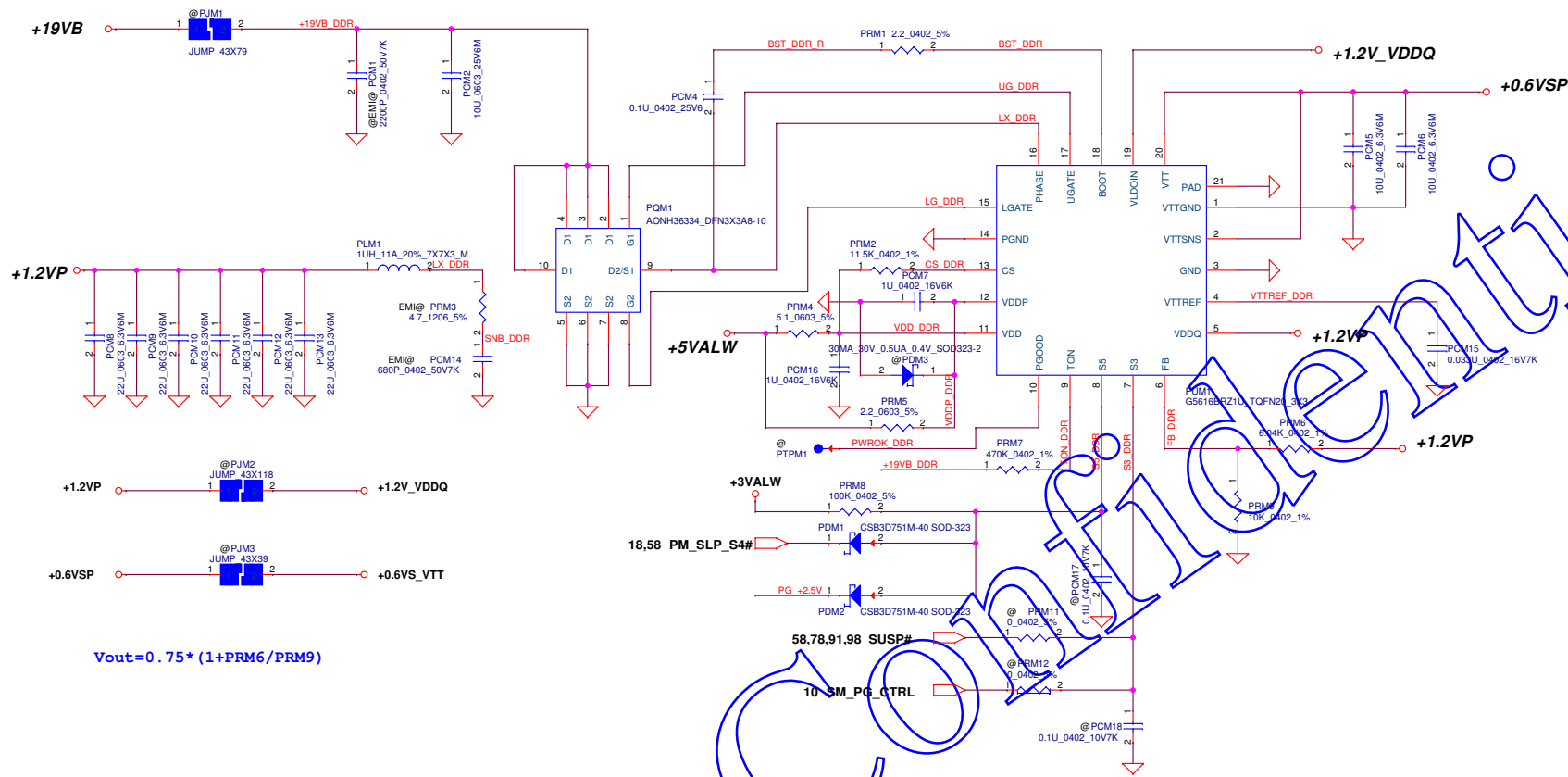
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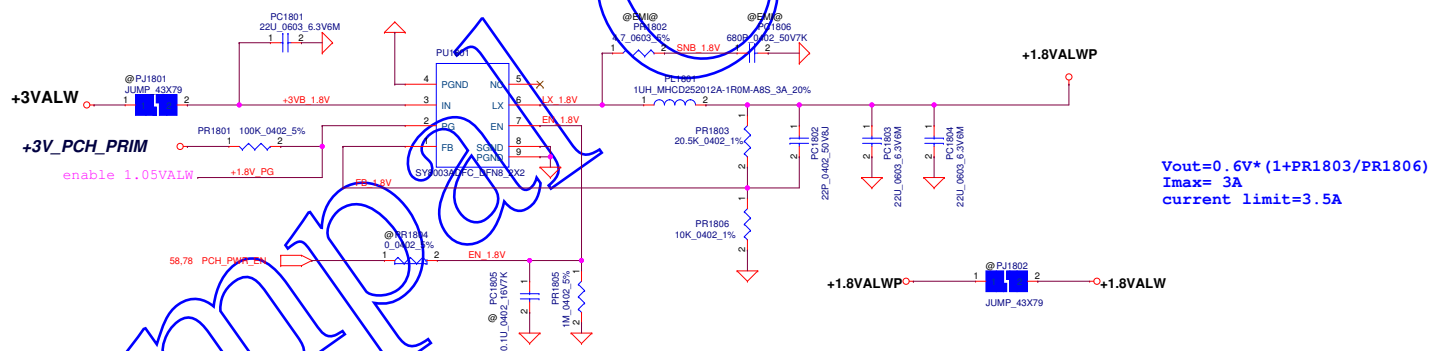
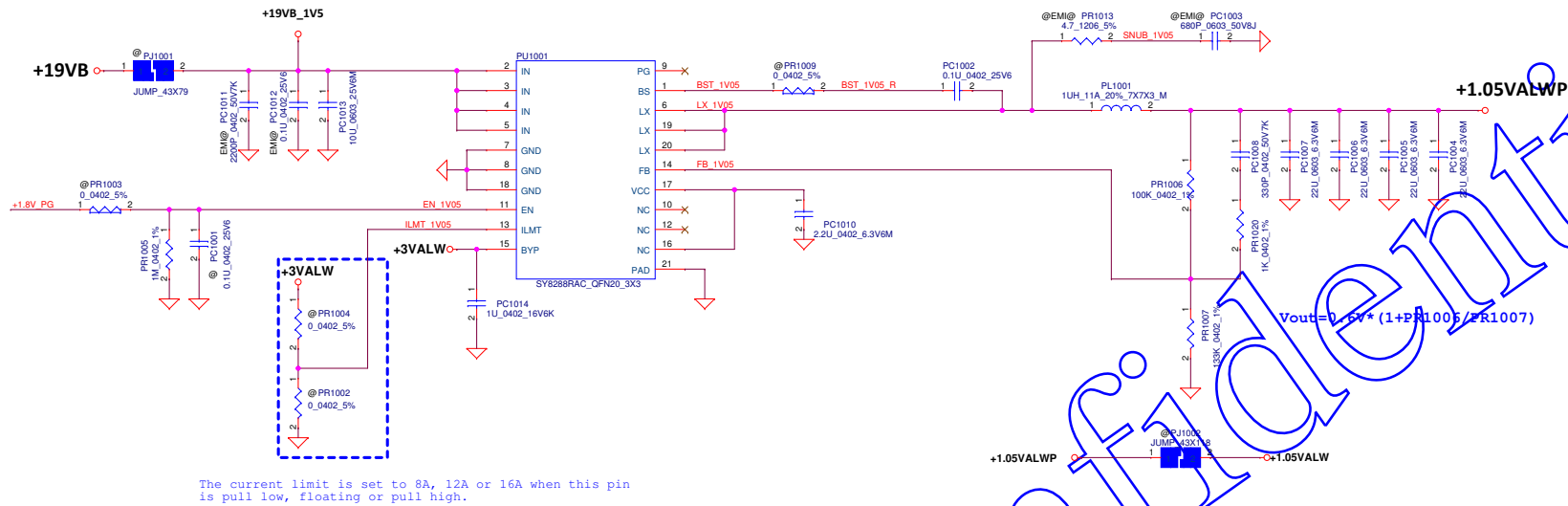
$$V_{out} = 0.75 \cdot (1 + PRM6/PRM9)$$

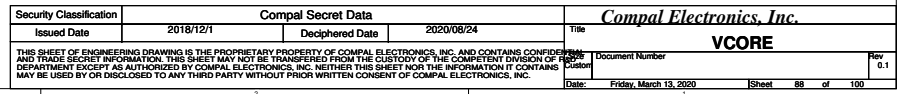
$$V_{out} = 0.6V \cdot (1 + PR2506/PR2507)$$

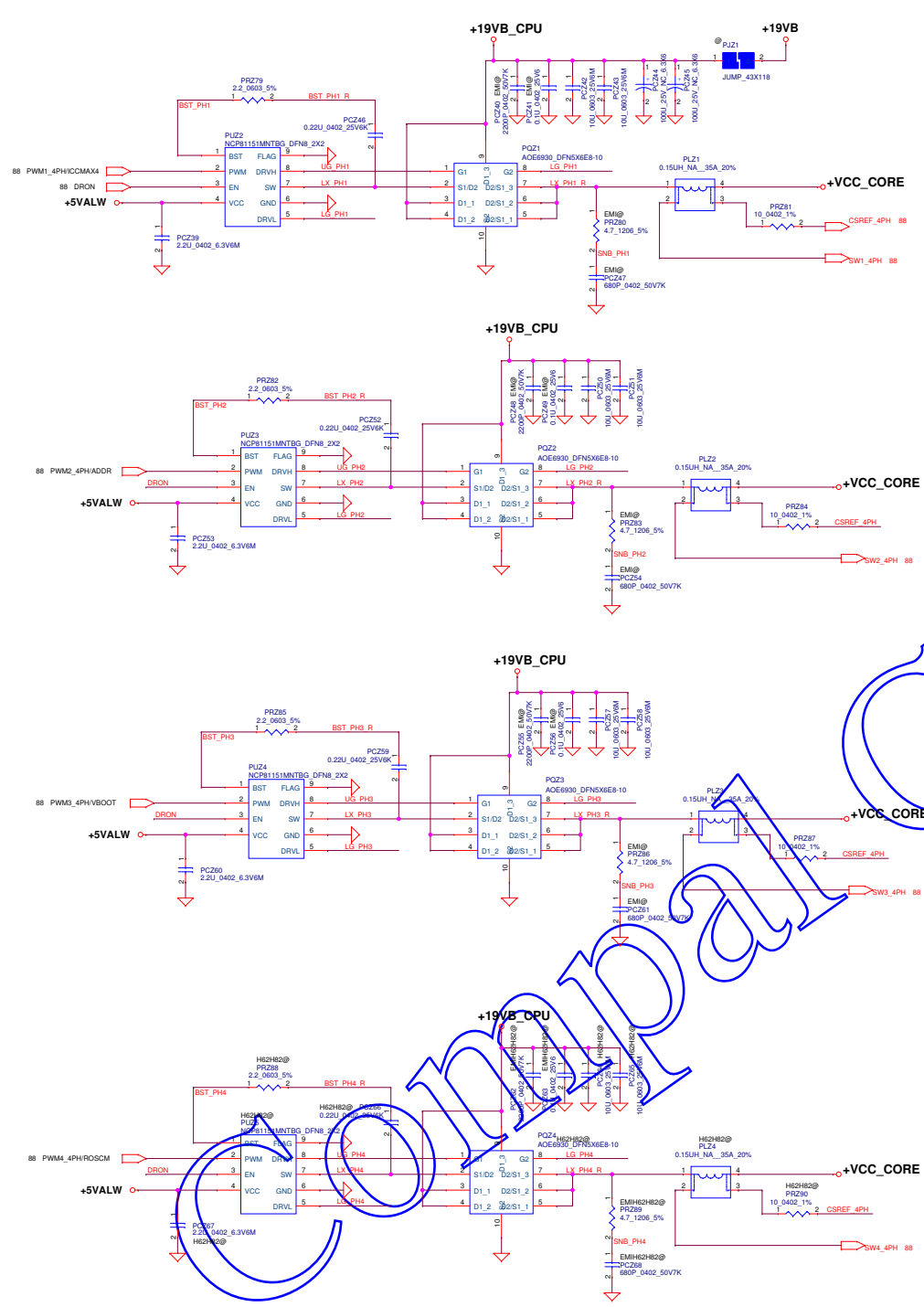
$$I_{max} = 2A$$

$$\text{current limit} = 3.5A$$

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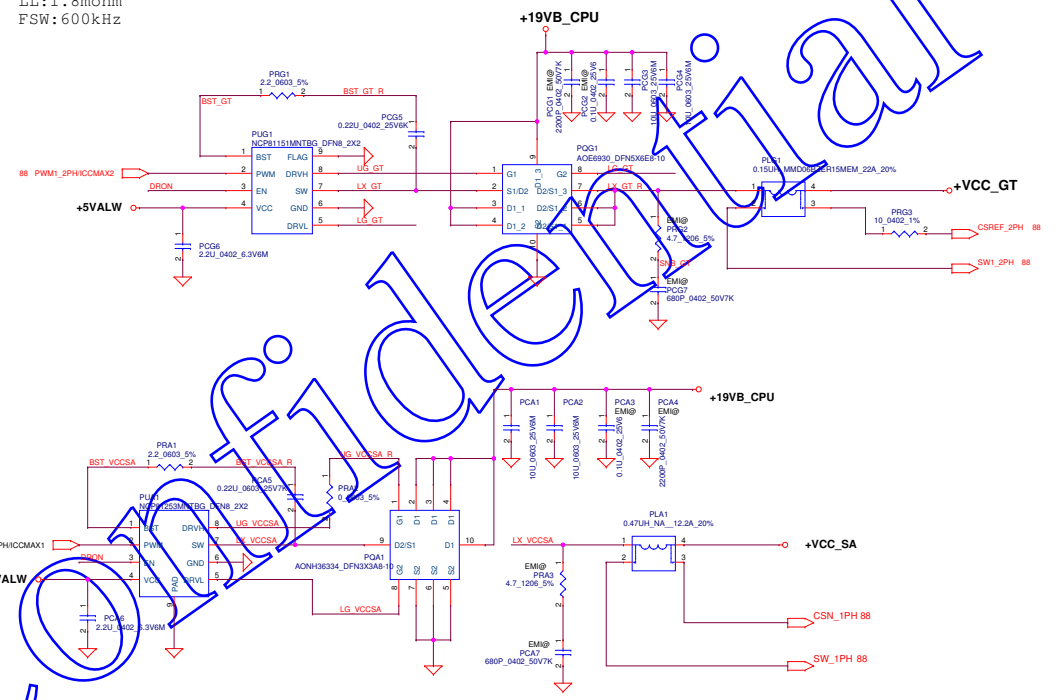




VCCORE
H82 ICCMAX:140A
H82 OCP:168A
H62 ICCMAX:128A
H62 OCP:168A
H42 ICCMAX:86A
H42 OCP:103A
LL:1.8mohm
FSW:600kHz

VCCGT
ICCMAX:32A
OCP:48A
LL:2.7mohm
FSW:600kHz

VCCSA
ICCMAX:11.1A
OCP:17.6A
LL:10.3mohm
FSW:600kHz



H42 IA
220u * 1
22u * 19
1u * 24

H62B IA
330u * 1
22u * 19
1u * 24

H62P IA
330u * 2
22u * 28
1u * 24

H42P IA
330u * 1
220u*1
22u * 22
1u * 24

GT
330u * 1
220u*1
22u * 8
1u * 12

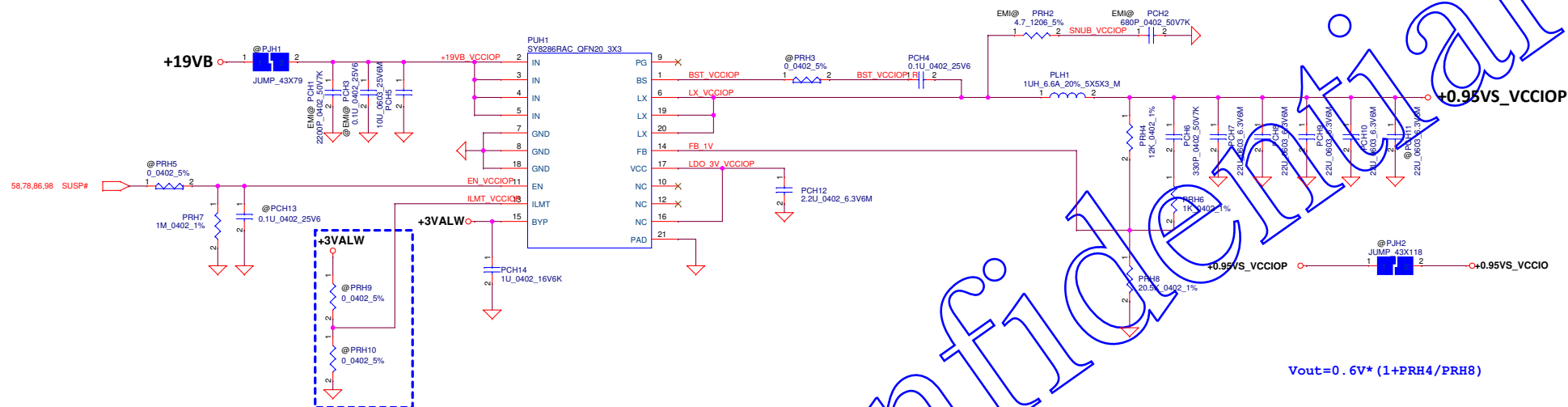
SA
22u * 7
1u * 1

+VCC_CORE

+VCC_GT

+VCC_SA

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					VCORE Decoupling
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The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

$$V_{out} = 0.6V * (1 + PRH4/PRH8)$$

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Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
 Rt=Rrefadj // (Rboot+Rref2)
 $V_{min} = V_{vref} * [R_{ref2} / (R_{ref2} + R_{boot})] * [R_t / (R_{ref1} + R_t)]$
 $V_{max} = V_{vref} * R_{ref2} / [(R_{ref1} / R_{refadj}) + R_{boot} + R_{ref2}]$
 $V_{out} = V_{min} + N * V_{step}$
 $V_{step} = (V_{max} - V_{min}) / N_{max}$

Module model information:
 RT8813D_V2A for IC module
 RT8813D_V2B for SW module

R1, R2, R3, R4, R5, C are
 based on VGA type to set.

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

PWM VID and Output voltage control
 1.Boot mode
 2.Standby mode (don't support)
 3.Normal mode

Switching frequency setting:
 $F_{sw} = (V_{in} - 0.5) / (2 * V_{in} * R_{ton} * 3.2p) = 352KHz$

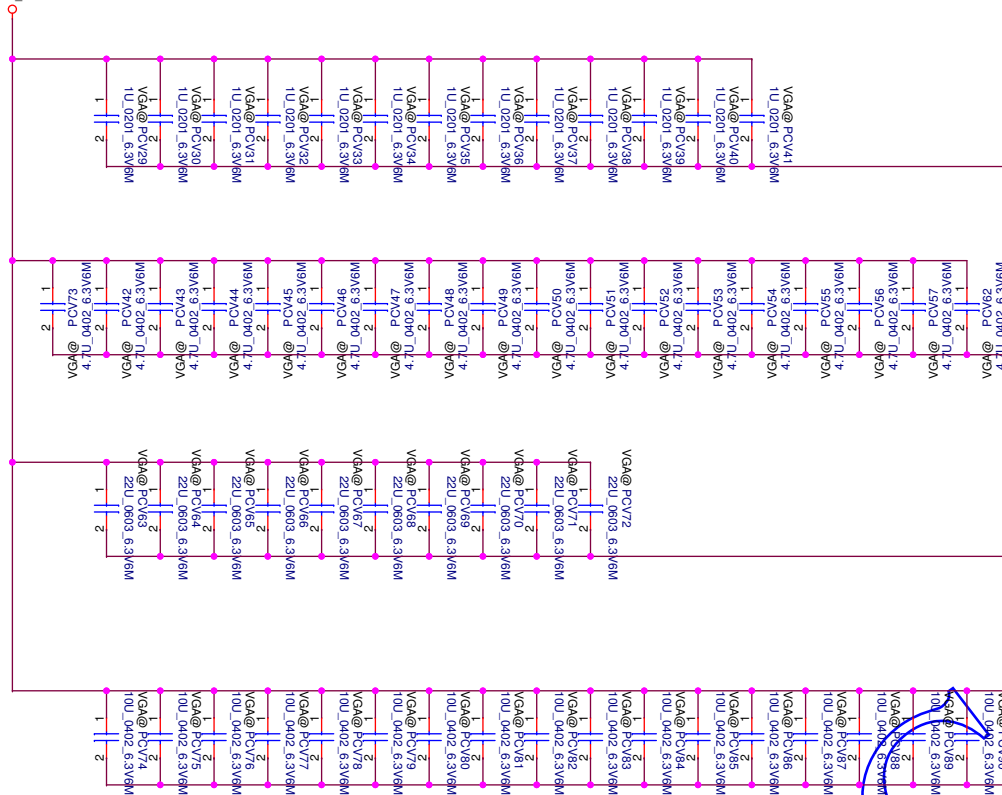
Current Limit threshold setting
 $R_{ocset} = (I_{valley} * R_{ds(on)} + 40mV) / I_{ocset}$

+VGA CORE
 EDP Continuous 59A/N17P-G0, 50A/N17P-G1
 EDP Peak 124A/N17P-G0, 90A/N17P-G1
 OCP: 130A
 Please base on GPU spec to calculate.

Please base on GPU spec to modify output cap.

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+VGA_CORE



+VGA_CORE
330uF X 4
4.7uF_0603X 18
22uF_0603 X 9
10uF_0603 X 16
1uF_0402X 13

Please base on GPU spec to modify output cap.

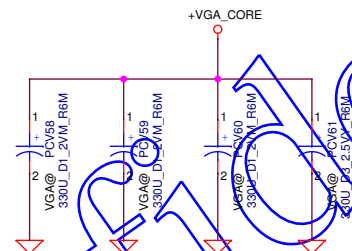
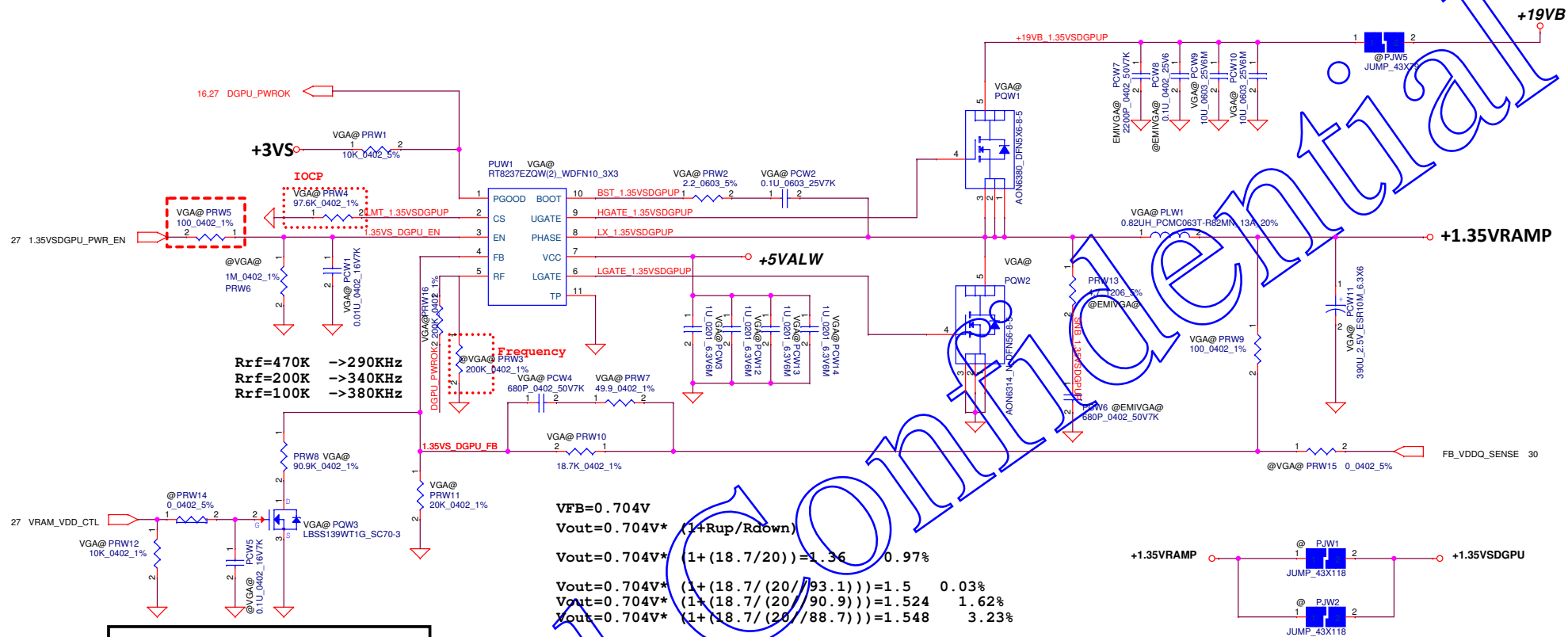
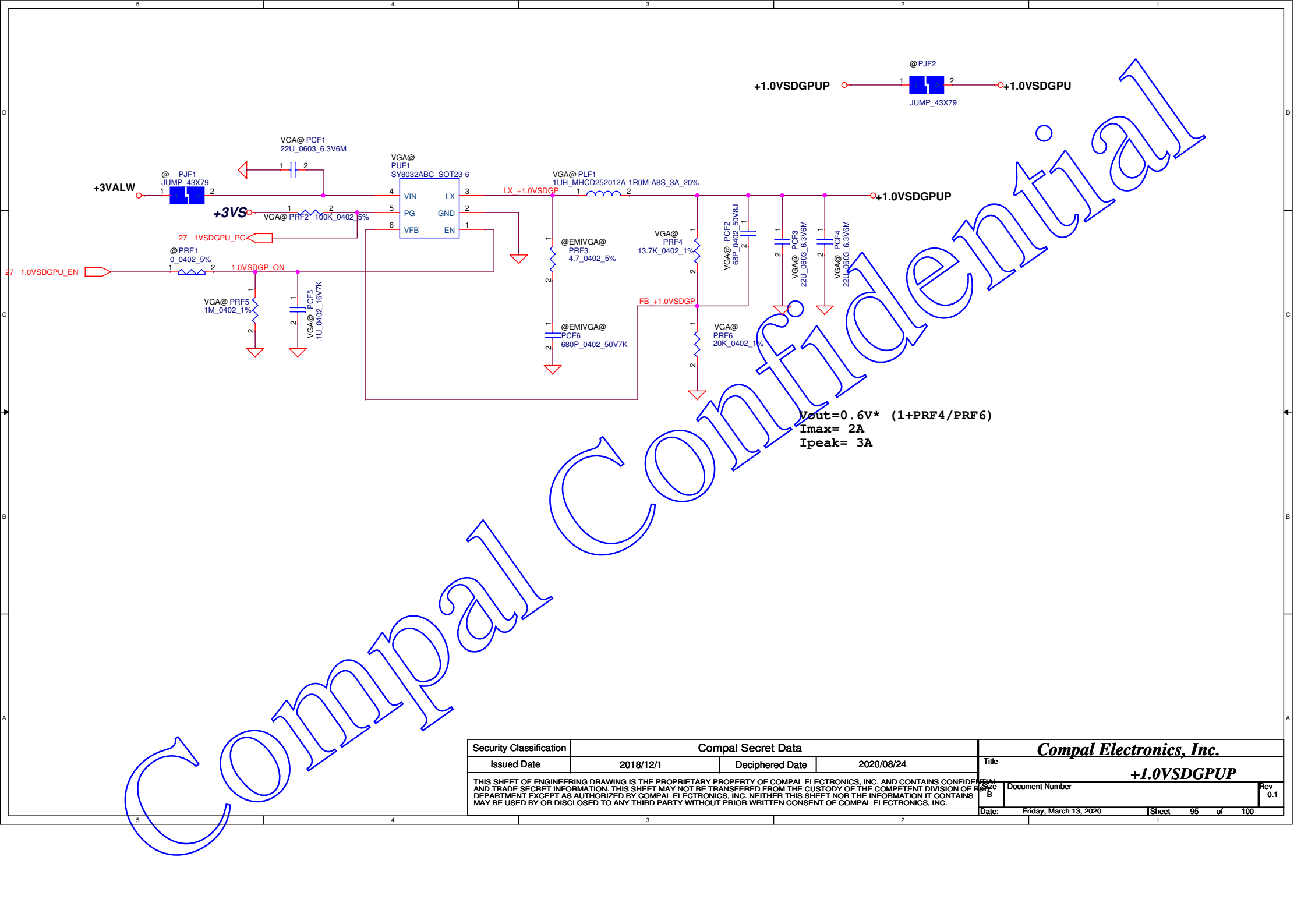


Table 7.17 GB4C-128 Package: Power Rail Filtering

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
NVVD		Varies	8 X 1uF (0402 X65) 16 X 4.7uF (0603 X65)	9 X 10uF (0603 X65) 7 X 22uF (0805 X65) 1 X 330uF (Poscap)
NVVD5		Varies	5 X 1uF (0402 X65) 5 X 10uF (0603 X65)	2 X 10uF (0603 X65) 3 X 22uF (0805 X65)





$V_{out} = 0.6V * (1 + PRF4 / PRF6)$
 $I_{max} = 2A$
 $I_{peak} = 3A$

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Item	Title	Change Description	Date
1	Charge design change	Change PCB13 from 55.46.0402 to 54.96.0402	2019/10/14
2	RIP Test requirements	Change PFI PFI from 25A0000100 to 25A00004500	2019/10/16
3	RIP Test requirements	Change PCB11 PCB11 from smpc to smp	2019/10/16
4	COMPAL source requirements	Change PCB15 from 28025681350 to 28024681100	2019/10/17

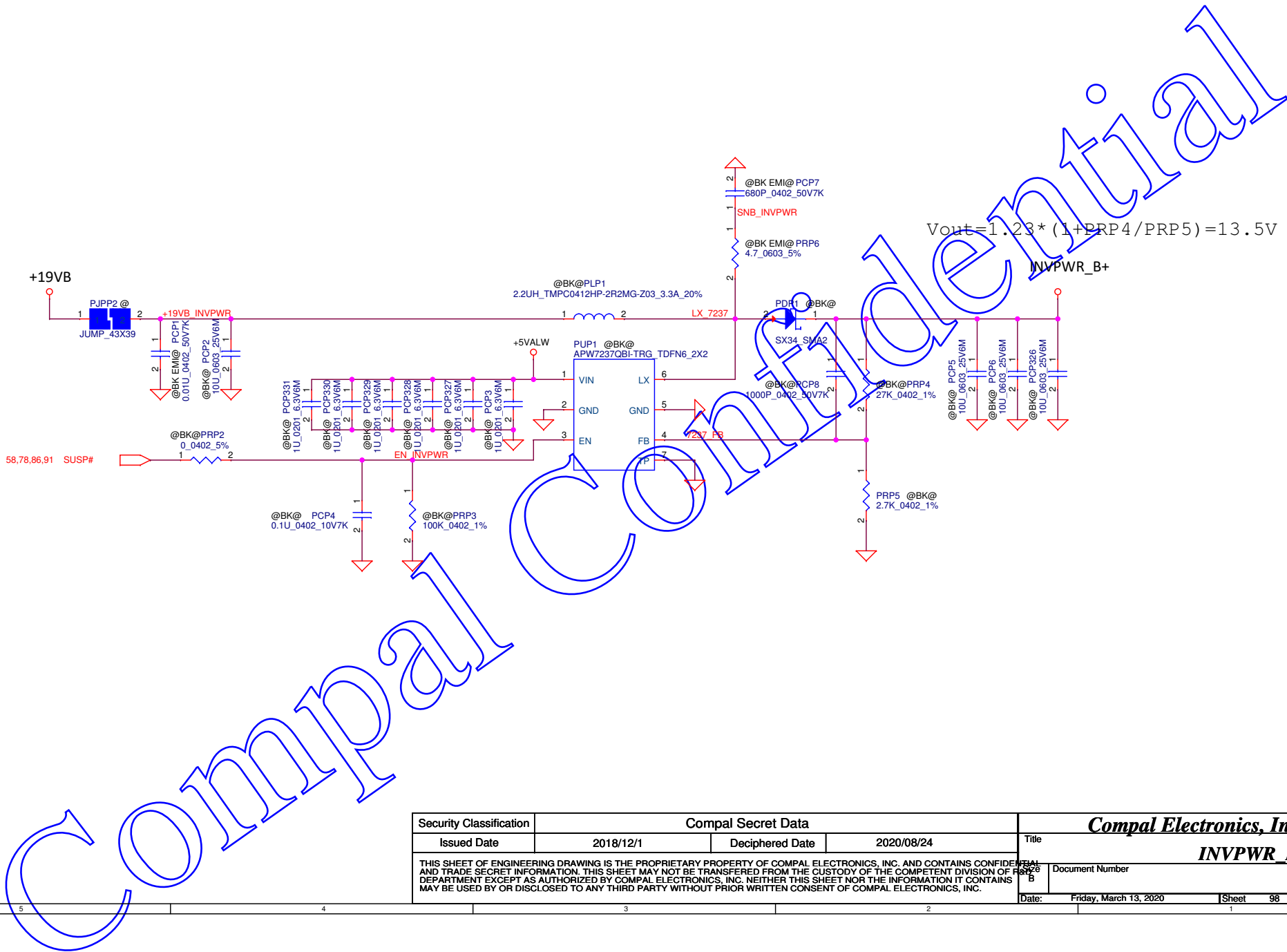
PV

Item	Title	Change Description	Date
1	CPU transient	Change PC277 from 25.5K to 27K(96GP)	2019/11/13
2	Charge design change	Change PCB25 from smp to smp	2019/11/13

SV

Item	Title	Change Description	Date
1	CPU transient	Change PC2172 from 220u to 330u(942)	2020/2/6

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